Noise Spectrum Notch Generation with Pulse Coding Control and EMI Noise Reduction Technology of DC-DC Switching Converter

YIFEI SUN

PhD Dissertation

DIVISION OF ELECTRONICS & INFORMATICS
GRADUATE SCHOOL OF SCIENCE & TECHNOLOGY
GUNMA UNIVERSITY

JAPAN

March 2020
Noise Spectrum Notch Generation with Pulse Coding Control

and EMI Noise Reduction Technology

of DC-DC Switching Converter

Dissertation
Submitted by

YIFEI SUN

In partial fulfillment of the requirements for the award of the Degree of

DOCTOR OF PHILOSOPHY
IN
ELECTRONICS & INFORMATICS ENGINEERING

Under the guidance of

PROFESSOR HARUO KOBAYASHI, Ph. D. Eng.

DIVISION OF ELECTRONICS & INFORMATICS
GRADUATE SCHOOL OF SCIENCE & TECHNOLOGY
GUNMA UNIVERSITY
JAPAN

March 2020
Acknowledgement

I would like to express my deepest appreciation to all those who provided me the possibility to complete this dissertation.

Special thanks to my supervisor Professor Dr. Haruo KOBAYASHI for his great guidance and encouragement. He not only taught me knowledge, but also taught me to become a good human. I would like to express my appreciation to Professor Yasunori KOBORI for his great guidance and advice. He promotes my internal motivation on research and encourages me to achieve the research goals with the right set of planning and measured steps. I would like to thank Professor Anna KUWANA for her kind advice. I would also like to thank Professors Masashi OCHIAI, Jun-ichi MATSUDA for valuable discussions. Additionally, I would like to thank Mr. Nobuyoshi ISHIKAWA for their help in procuring lab equipment and managing funding.

I am thankful to the members of our Laboratory. Thanks to Jianlong WANG for his valuable help on my research and daily life. Thanks to Tran MINH TRI, Noriyuki OIWA, Shogo KATAYAMA for their valuable discussion and advice. Thanks to Jing LI, Dan YAO, Shiyu WANG, Yujie ZHAO for their help in my Japanese communication. I would also like to thank Rino TAKAHASHI, as my Japanese tutor, her teach me Japanese language and culture.

I was greatly assisted by the Gunma University Human Resources Cultivation Center as a research assistant from 2018-2020. Thanks to Prof. Kenichi KASUYA, Prof. Kuniyuki MOTOJIMA, Coordinator Kumiko TAURA and Seretary Nami SAKAGUCHI.

Furthermore, I would like to thank my alma mater Shenyang University of Chemical Technology and Professor Decheng YUAN who is my master degree supervisor, who gives me the opportunity to go abroad, learning advanced technology, given me a rational look at the world.

Finally, sincerely thank to my parent Mei LI and Rong SUN. Thanks for their endless love and all that they did for me. Thanks to Zhe XU, who gives me courage and spiritual support.
Declaration

I hereby declare that this submission is my own work and that, to the best of my knowledge and belief, it contains no material previously published or written by another person, nor material which has been accepted for the award of any other degree of the university or other institute of higher learning, except where due acknowledgement has been made in the text.

Signature:

Name: YIFEI SUN

Student No.: 

Date:
Abstract

This dissertation deals with the reduction of Electromagnetic Interference (EMI) in the DC-DC switching converter for the communication equipment. Simultaneously, a novel EMI spread spectrum technology is proposed that does not distribute the switching noise into some specified frequency bands.

For reducing the switching noise of DC-DC switching converter, we often use frequency modulation of the clock. But in the hysteretic control converter with Constant-On Time (COT) pulse and ripple injection method or soft switching converter, there is no fixed clock pulse. For these clock-less switching converter, we have developed techniques to reduce EMI noise. In this case, the modified ripple is also increased and it is corrected by developed ripple reduction method.

In the Pulse Width Modulation (PWM) method for switching converter also causes EMI noise on its clock frequency and harmonics. In order to reduce the EMI noise, modulation of the clock pulse is used by shaking the phase or frequency of the clock. Since the energy of clock frequency and its high frequency harmonics can be diffused to other frequencies, the peak level of the clock spectrum is low and there is no line spectrum at the frequency of the clock and its harmonic spectra, but the bottom level (floor noise) is high. Therefore, we have created an EMI spread spectrum technique with both EMI reduction and noise diffusion based on Spread-Spectrum Clock Generator (SSCG) uses a Delta-sigma (ΔΣ) Digital-to-Time Converter (DTC) to spread the clock spectrum while allowing us to select the bands that we do not want to spread by predecessors.

In this dissertation we propose an EMI spread spectrum technology with automatically setting of the notch frequency using the pulse coding controlled method in the DC-DC switching converter for the communication equipment. In communication devices, small noise as much as possible is desired at the receiving signal band. We realized the method that notch frequency can be automatically set to the frequency of the received signal by adjusting the clock frequency. Therefore, just let the notch frequency be equal to the received signal frequency suppress noise in the received signal frequency.

Chapter 1 introduces the background, the motivation, and the objectives of this research and the proposed approaches. Chapter 2 discusses the basic topology and basic operation of DC-DC switching converter. Chapter 3 presents proposed EMI reduction and output ripple suppression method. Chapter 4 discusses notch frequency method
with pulse coding control in switching converter. Chapter 5 describes a full-automatic notch generation of pulse width coding switching converter. Chapter 6 confirmed the notch frequency experimentally with the prototype circuit. Chapter 7 summarizes conclusions obtained through this research and future work is proposed.
# Contents

Acknowledgement ........................................................................................................... I
Declaration......................................................................................................................... II
Abstract............................................................................................................................. III
Contents ............................................................................................................................ V
List of Figures ..................................................................................................................... VIII
List of Tables ...................................................................................................................... XIII
1. Introduction ................................................................................................................ 1
   1.1 Research background .......................................................................................... 1
   1.2 SSCG for Switching Converter using Digital $\Delta\Sigma$ Modulation ....................... 3
      1.2.1 SSCG using PWM $\Delta\Sigma$ DTC ................................................................. 3
      1.2.2 Notch Frequency Generation due to Two-Coding Pulse ............................... 6
   1.3 Organization of Dissertation ................................................................................ 7
2. Conventional DC-DC Switching Converter ............................................................... 8
   2.1 Basic Topology .................................................................................................... 8
   2.2 Basic Operation of DC-DC Switching Converter ................................................. 11
      2.2.1 Basic Operation of Buck Converter ............................................................. 11
      2.2.2 Power Stage Transfer Function of Buck Converter ..................................... 15
      2.2.3 Boost Converter .......................................................................................... 20
      2.2.4 Buck-boost converter .................................................................................. 22
   2.3 Hysteretic Control Switching Converter ............................................................. 25
      2.3.1 Basic Operation of Hysteretic Control Converter ......................................... 26
      2.3.2 Features of Hysteretic Control Converter .................................................... 27
      2.3.3 COT Type Hysteretic Control Converter ...................................................... 28
      2.3.4 Ripple Injection Method of Hysteretic Control Converter ............................ 30
   2.4 Soft Switching Converter ..................................................................................... 31
      2.4.1 Features of Soft Switching Converter .......................................................... 31
      2.4.2 Basic Operation of Soft Switching Converter .............................................. 33
   2.5 Summary .............................................................................................................. 35
3. EMI Noise Reduction Technology .............................................................................. 36
   3.1 EMI Reduction with PWM Control Converter .................................................... 38
      3.1.1 Conventional EMI Noise with PWM Control Buck Converter .................... 38
      3.1.2 EMI Noise Reduction with Clock Frequency Modulation ............................ 40
      3.1.3 EMI Reduction & Output Ripple Improvement ............................................ 41
3.2 EMI Reduction with Hysteretic Control Converter

3.2.1 Conventional Hysteretic Control Converter using COT Method

3.2.2 EMI Noise Reduction with COT Control Method

3.2.3 Improved EMI Noise Reduction with COT Control Method

3.2.4 Conventional EMI Noise Reduction with Ripple Injection Method

3.2.5 EMI Reduction and Output Ripple Improvement with Ripple Injection Method

3.3 EMI Reduction with Soft-Switching Converter

3.3.1 Conventional Soft-Switching Converter

3.3.2 EMI Reduction with Soft-Switching Converter

3.3.3 Output Ripple Cancelation with EMI Reduction

3.4 Summary

4. Notch Frequency with Pulse Coding Control

4.1 Pulse Width Coding (PWC) Control Switching Converter

4.1.1 PWC Method Switching Converter

4.1.2 Simulation Result with the PWC Control

4.2 Pulse Phase Coding (PPC) Control Switching Converter

4.3 Pulse Cycle Coding (PCC) Control Switching Converter

4.3.1 PCC Method Switching Converter

4.3.2 Simulation Result with the PCC Control

4.4 Pulse Width and Phase Coding (PWPC) Control Switching Converter

4.4.1 PWPC Method Switching Converter

4.4.2 Simulation Result with the PWPC Control

4.5 Derivation of Theoretical Notch Frequency

4.5.1 Theoretical Analysis of PWC Method

4.5.2 Theoretical Analysis of PPC and PCC Method

4.5.3 Theoretical Analysis of PWPC Method

4.6 Summary

5. Full-Automatic Notch Generation of PWC Switching Converter

5.1 Automatic Notch Frequency Generation with PWC Control

5.1.1 Best Relationship Between Fck and Fn

5.1.2 Automatic Notch Frequency Generate from Clock Pulse

5.1.3 Simulation Results with Automatic Notch Frequency Generation

5.1.4 Automatic Setting Notch Frequency According to Input Frequency

5.2 Automatic Notch Frequency Generation with PWPC Control

5.2.1 Automatic Method to Generate PWPC Control
5.2.2 Simulation Results with Automatic Notch Frequency Generation with PWPC Control

5.3 Automatic Design of Duty Ratio D in Full Automatic Notch Frequency Generation

5.3.1 Analysis Relationship Between Conversion Voltage Ration and PWM Duty Ratio

5.3.2 Simulation Result with Influence of D Change

5.3.3 Optimal D Setting Method

5.3.4 Automatic Detection of PWM Duty Method

5.4 Summary

6. Implementation Evaluation on Pulse Coding Controlled Switching Converter with Notch Frequency Generation

6.1 Notch Frequency Generation Experimental of the PWC Method Switching Converter

6.1.1 Experimental Method of PWC Control Switching Converter

6.1.2 Experimental Result of the PWC Converter

6.2 Experimental of Automatic Notch Frequency Generation

6.2.1 Experimental Method of Automatic Notch Frequency Generation

6.2.2 Experimental Result of Automatic Notch Frequency Generation

6.3 Summary

7. Conclusion

7.1 Conclusion

7.2 Items for the Future Study

Bibliography

List of Published Papers

Journal Papers

International Conference Papers

Domestic Conferences / Seminars

Award
List of Figures

Figure 1.1 Circuit structure of spread spectrum clock generator .............................. 4
Figure 1.2 Spectrum of pulse coding signal. .......................................................... 5
Figure 1.3 Modulation figures of PWM. ................................................................. 6
Figure 1.4 PWM pulse sequence. ........................................................................... 6
Figure 1.5 Spectrum of PWM using PWM ΔΣ DTC. .............................................. 7
Figure 2.1 Performance of DC-DC switching converter. ........................................ 9
Figure 2.2 Basic configuration of DC-DC switching converter. .............................. 10
Figure 2.3 Basic constitution of buck, boost, and buck-boost converters. ............ 10
Figure 2.4 Switch state and switching waveform..................................................... 11
Figure 2.5 Basic circuit of buck converter............................................................... 12
Figure 2.6 Buck converter when switch (SW) turns on. .......................................... 12
Figure 2.7 Buck converter when switch (SW) turns off. ......................................... 13
Figure 2.8 Timing chart of buck converter (continuous current mode (CCM)) ..... 13
Figure 2.9 Voltage-mode negative feedback control circuit................................. 14
Figure 2.10 Waveforms in switching converter....................................................... 14
Figure 2.11 Basic circuit of power stage. ............................................................... 15
Figure 2.12 On-period equivalent circuit .............................................................. 16
Figure 2.13 Off-period equivalent circuit ............................................................. 16
Figure 2.14 CCM block diagram of buck converter................................................ 19
Figure 2.15 Bode diagram of the buck converter. .................................................. 20
Figure 2.16 Basic circuit of the boost converter...................................................... 21
Figure 2.17 Boost converter when switch (SW) turns on. ....................................... 21
Figure 2.18 Boost converter when switch (SW) turns off. ....................................... 22
Figure 2.19 Timing chart of the boost converter (CCM)......................................... 22
Figure 2.20 Basic circuit of the buck-boost converter........................................... 23
Figure 2.21 Buck-boost converter when switch (S) turns on. ................................. 24
Figure 2.22 Buck-boost converter when switch (S) turns off. ............................... 24
Figure 2.23 Timing chart of the buck-boost converter. .......................................... 25
Figure 2.24 Basic hysteretic control buck converter. ............................................. 26
Figure 2.25 Operation waveforms of hysteretic control........................................ 27
Figure 2.26 COT type hysteretic control buck converter. ..................................... 29
Figure 2.27 Timing chart of COT type hysteretic control buck converter............... 29
Figure 2.28 Ripple injection method buck converter. ............................................ 30
Figure 2.29 Waveforms of ripple injection converter .................................................. 31
Figure 2.30 Voltage and current during hard switching (a): off-process (b): on-process .......................................................... 32
Figure 2.31 Voltage and current during soft switching (a): off-process (b): on-process .......................................................... 32
Figure 2.32 Full-wave resonant soft-switching ......................................................... 34
Figure 2.33 Timing chart of full-wave resonant soft-switching .................................. 34
Figure 3.1 Waveforms analysis of a frequency-hopped buck converter with two hopping frequencies ........................................................................... 37
Figure 3.2 EMI regulation in radiation noise (CISPR22) in Japan ................................. 38
Figure 3.3 Buck converter with PWM signal control .................................................... 39
Figure 3.4 Simulated spectrum without EMI reduction ................................................ 39
Figure 3.5 Frequency modulation of buck converter with PWM signal control ......... 40
Figure 3.6 Spectra of modulation converter .............................................................. 41
Figure 3.7 Output ripple with/without modulation ...................................................... 41
Figure 3.8 SAW generator & modified current source .................................................. 43
Figure 3.9 Comparison of SAW signals ..................................................................... 43
Figure 3.10 Modulated and corrected ripple ............................................................... 44
Figure 3.11 COT control method hysteretic control converter ...................................... 46
Figure 3.12 Waveforms of COT type hysteretic control converter ......................... 46
Figure 3.13 EMI noise reduction with COT control circuit ........................................ 47
Figure 3.14 Timing chart of modified COT pulse ....................................................... 47
Figure 3.15 COT control method spectrum without EMI reduction ....................... 48
Figure 3.16 Spectrum with EMI reduction ................................................................. 49
Figure 3.17 Output ripple with modulation ............................................................... 49
Figure 3.18 Improved EMI noise reduction with the COT control method ............. 50
Figure 3.19 Block diagram of improved EMI noise reduction with the COT converter. ............................................................................. 50
Figure 3.20 Output ripple with improved EMI noise reduction with the COT converter ................................................................................. 51
Figure 3.21 EMI noise reduction with the ripple injection method ......................... 52
Figure 3.22 Spectrum of the ripple injection method hysteretic converter ............ 52
Figure 3.23 Circuit to cancel the output ripple ......................................................... 54
Figure 3.24 Cancellation of the output ripple ............................................................ 54
Figure 3.25 Cancellation of the ripple $V_{oc}$ .............................................................. 55
Figure 3.26 Signals with cancellation ....................................................................... 55
Figure 3.27 Circuit of the full-wave resonant converter.............................. 56
Figure 3.28 EMI reduction modulation circuit........................................... 57
Figure 3.29 Simulation waveforms in EMI reduction modulation circuit........ 57
Figure 3.30 Spectrum of the soft-switching converter output........................ 58
Figure 3.31 Spread spectrum of the soft-switching converter output............... 59
Figure 3.32 Waveforms in the ripple cancellation circuit.............................. 60
Figure 3.33 Circuit of the output ripple cancellation method.......................... 60
Figure 3.34 Output ripple with EMI reduction (red) and ripple cancellation (green).
................................................................................................................. 61
Figure 3.35 ZVS operation waveforms at ripple correction............................ 62
Figure 3.36 ZVS operation improvement circuit. ......................................... 62
Figure 3.37 Waveforms of ZVS operation improvement............................... 62
Figure 3.38 Simulation result of the resonant voltage improvement............... 63
Figure 3.39 Spectrum of ZVS improvement circuit....................................... 63
Figure 4.1 Switching converter with pulse coding....................................... 66
Figure 4.2 Buck converter with PWC control............................................. 67
Figure 4.3 Main signal waveforms of PWC method..................................... 67
Figure 4.4 Main signal waveforms of PWC method..................................... 69
Figure 4.5 Spread spectrum with PWC control.......................................... 69
Figure 4.6 Transient response characteristics of PWC method...................... 69
Figure 4.7 Buck converter with PPC control.............................................. 70
Figure 4.8 Waveforms of PPC control........................................................ 71
Figure 4.9 Coded pulses with the PCC method.......................................... 72
Figure 4.10 Buck converter with PCC control............................................ 73
Figure 4.11 Main signal waveforms of PCC method.................................... 73
Figure 4.12 Simulation waveforms of PCC method..................................... 74
Figure 4.13 Spectrum of buck converter with PCC control (without EMI reduction).
................................................................................................................. 74
Figure 4.14 Buck converter with PWPC control.......................................... 75
Figure 4.15 Main signal waveforms of PWPC method................................. 76
Figure 4.16 Spectrum of buck converter with PWPC control......................... 76
Figure 4.17 Transient response characteristics of PWPC method................... 77
Figure 4.18 1 period 2 pulse trains of pulse width coding signal..................... 77
Figure 4.19 1 period 8 pulse trains of pulse width coding signal..................... 79
Figure 4.20 Comparison diagram between theoretical formula and spectrum... 80
Figure 4.21 1 period 2 pulse trains of pulse phase coding signal.................... 80
Figure 4.22 1 period 2 pulse trains of pulse cycle coding signal. .................................. 81
Figure 4.23 1 period 4 pulse trains of pulse width pulse phase coding signal. .......... 82
Figure 4.24 Comparison of notch characteristics with PWC method and PWPC method. .................................................................................................................. 83
Figure 5.1 Best position of $F_n$ occurrence ................................................................. 86
Figure 5.2 Timing chart of relationship between Pulse-H and Pulse-L of PWM signals. ...................................................................................................................... 87
Figure 5.3 Pulse coding of automatic PWC method in $P = 1$ situation. ................. 88
Figure 5.4 Pulse coding of automatic PWC method in $P = N$ situation ................. 89
Figure 5.5 Simulation waveforms of Pulse-L and Pulse-H generation in $P = 1$ situation. ................................................................................................................. 90
Figure 5.6 Simulated spectrum by PWM signal without EMI reduction when $P = 1$ situation. .......................................................................................................... 90
Figure 5.7 Simulated spectrum with EMI reduction in $P = 1$ situation. ............... 91
Figure 5.8 Simulation waveforms of pulse-H and pulse-L generation in $P = 2$ situation. ................................................................................................................. 92
Figure 5.9 Simulated spectrum with EMI reduction in $P = 2$ situation. ............... 92
Figure 5.10 Simulation waveforms of Pulse-H and Pulse-L generation in $P = 3$ situation. ................................................................................................................. 93
Figure 5.11 Simulated spectrum with EMI reduction in $P = 3$ situation. ............... 93
Figure 5.12 Block of change channel 1 to channel 2 ...................................................... 94
Figure 5.13 $F_{in1} = 750kHz$ situation ........................................................................... 94
Figure 5.14 $F_{in2} = 1,250kHz$ situation ........................................................................ 95
Figure 5.15 Automatic switching on transient response and saw-tooth ............... 96
Figure 5.16 Pulse coding of PWPC method ................................................................. 97
Figure 5.17 Timing chart of buck converter with PWPC control ............................. 97
Figure 5.18 Waveforms of saw-tooth with period $T_{ck}$ and delay $T_{ck}$ .............. 98
Figure 5.19 Main waveforms of PWPC method ........................................................... 99
Figure 5.20 Simulated spectrum with EMI reduction using PWPC method .......... 99
Figure 5.21 Waveforms of the SEL signal ................................................................. 102
Figure 5.22 Change of the output voltage ripple ...................................................... 103
Figure 5.23 Waveforms of the select signal and ripple of output voltage in $D=0.28$ situation. ............................................................................................................ 103
Figure 5.24 $D$ automatic detection circuit ................................................................. 105
Figure 5.25 Main signal waveforms of $D$ detection method .................................... 105
Figure 5.26 Simulated spectrum with full automatic notch frequency generation
without EMI reduction. ................................................................. 106
Figure 5.27 Select signal waveform with full automatic notch frequency generation.
.............................................................................................. 106
Figure 5.28 Output voltage ripple with full automatic notch frequency generation.
.............................................................................................. 106
Figure 6.1 Converter with PWC control.................................................. 109
Figure 6.2 The flowchart for using Kicad software.................................. 110
Figure 6.3 PWC control buck converter circuit with Kicad...................... 111
Figure 6.4 PWC control buck converter PCB board.................................. 112
Figure 6.5 Waveforms of $WH$ and $WL$ in PWC control buck converter. ...... 113
Figure 6.6 Spectrum of the PWC control switching converter.................. 113
Figure 6.7 Automatic notch frequency generation circuit with Kicad......... 114
Figure 6.8 Main signal waveforms when using $Tin$ create $Tck$.................. 115
Figure 6.9 Automatic notch frequency generation PCB board circuit.......... 116
Figure 6.10 Experimental waveforms of $WH$ and $WL$ ($Fin = 400kHz$)........ 117
Figure 6.11 Experimental waveforms of PWM and SEL signals ($Fin = 400kHz$).
................................................................................................. 117
Figure 6.12 Simulation spectrum of PWM signal ($Fin = 400kHz$).............. 118
Figure 6.13 Experimental spectrum of PWM signal ($Fin = 400kHz$).......... 118
Figure 6.14 Experimental waveforms of $WH$ and $WL$ ($Fin = 600kHz$)........ 119
Figure 6.15 Experimental waveforms of PWM and SEL signals ($Fin = 600kHz$).
................................................................................................. 119
Figure 6.16 Simulation spectrum of PWM signal ($Fin = 600kHz$).............. 119
Figure 6.17 Experimental spectrum of PWM signal ($Fin = 600kHz$).......... 120
Figure 6.18 Transient response characteristics of the PWC method............. 120
List of Tables

Table 2.1 Parameters of the buck converter .................................................. 20
Table 3.1 Parameter values of simulation circuit ........................................... 40
Table 3.2 Simulation parameters ................................................................. 43
Table 3.3 Simulation parameters ................................................................. 45
Table 3.4 Parameter values in simulation ..................................................... 58
Table 4.1 Parameter values of PWC control simulation circuit ....................... 68
Table 4.2 Parameter values of PCC control simulation circuit ....................... 74
Table 6.1 Parameter values of implementation circuit ................................... 112
Table 6.2 Parameter values of implementation circuit ................................... 116
1. Introduction

This dissertation describes the results of research on an EMI reduction in the DC-DC switching converter for the communication equipment. Furthermore, we propose a spread spectrum technology that the noise component of a specific frequency could be suppressed. In this chapter, first we introduce the research background. Next, based on the background, we describe how predecessors notice that the notch characteristics appears in the spectrum of the output pulse in the pulse coding system in DTC circuit [1]. Then, the motivation and purpose of this dissertation are explained. The organization of the dissertation is shown in the last section in this chapter.

1.1 Research background

In recent years, switching power supply circuits are used in many electronic devices because of their advantages such as high efficiency, high performance (such as low output ripple and fast transient response), large current output and continuously variable output voltage. Also the communication circuit has been accelerated to be powerful and higher density packaging. However, since the switching power supply circuit is driven by switch with the clock, it will generate large switching noise [2]-[3]. The fluctuation of the switching noise has strongly spread in the wide frequency range with the acceleration of high-speed and high-frequency electronic equipment. So it is very important to reduce EMI noise.

EMI stands for electromagnetic interference. In terms of switching power supplies, the action of switching generates switching noise. In a loop in which currents are suddenly turned on and off during switching, high-frequency ringing (switching noise) occurs due to parasitic components. In order to reduce the switching noise that they generate, complex noise filtering and shielding are needed which make the switching power supply larger in size and costly [4]. For this reason, noise reduction methods that do not use filters are required in many fields, including the automotive field. There are some techniques for broadening and flattening their switching noise power spectrum to reduce EMI and to satisfy EMI regulation [5], such as spread spectrum method that randomly modulates the clock signal [6]-[9]. Spread spectrum of switching power supply means changing the switching frequency in a certain range and distributing noise energy to surrounding frequencies without concentrating on one frequency, lowering the
peak value of noise and clearing EMI standards, generating noise. The technique to reduce the impact on the equipment such as spread spectrum method that randomly modulates the clock signal is being used. For example, some techniques talk about EMI reduction method with spread spectrum using pseudo analog noise which is produced from M-sequence circuit with PLL circuit [10]. Some techniques talk about digital pseudo-random dithering of the switching, regulator control clock timing, and such clock jitter can be introduced by adding simple digital circuitry [11]. Some techniques talk about using triangular waveform modulation as the spectrum modulation method. Moreover, some spread spectrum methods talk about chaos-based pulse width modulation [12]-[17].

Although these methods suppressing the peak levels at the fundamental frequency and its harmonic frequencies, there are problems such as ripple of output voltage will increase or the diffusion noise is superimposed on an unwanted band (diffusion band). Particularly, in the automobile field, the density and complexity of internal electronic circuits are progressing toward electrification and automatic driving. If EMI countermeasures are not taken, noise may be superimposed on the radio band or malfunctions may be induced in other electronic devices. Vehicle noise standards are stricter than consumer products. Not only is the standard itself strict, but it is also required that AM radio sound must not contain noise. For this reason, the switching frequency of the DC-DC converter is preferably 2MHz or higher, which is higher than the AM radio frequency band, but this leads to a demand for high-speed switching and causes further high-frequency noise. In response to EMI standards for in-vehicle equipment, many countermeasures are required. One example of this is that “the switching frequency used in in-vehicle DC-DC converters and their high frequencies must not overlap with the reception frequency band of radio AM, FM” [18].

So we try to consider about some spread spectrum techniques for EMI reduction with suppressing diffusion of power supply noise and decrease output ripple. Moreover, we propose a spread spectrum technique for clock pulse with suppressing diffusion of power supply noise using pulse width coding methods, based on the notch characteristics design. We expect that if notch frequency is set to the frequency of the received signal by adjusting the clock frequency. Therefore, just let the notch frequency be equal to the received signal frequency, it will suppress noise in the received signal frequency and be not affected by other spread spectrum. So in the following part, it will be shown that the occurrence of the notch characteristic by predecessors is the motivation of this research.
1.2 SSCG for Switching Converter using Digital $\Delta \Sigma$ Modulation

Predecessors have suggested an auto-configurable Spread-Spectrum Clock Generator (SSCG) that dynamically changes clocks spread spectrum in a way to eliminate clock speeded collision with other desired signal in neighboring frequency bands. This proposed method uses a Delta-Sigma ($\Delta \Sigma$) Digital-to-Time Converter (DTC) to spread the clock spectrum while allowing us to select the bands that we do not want to spread.

1.2.1 SSCG using PWM $\Delta \Sigma$ DTC

Constant trend of device miniaturization and functioning frequency has led to rise in $\Delta \Sigma$ modulation methods popularity. The usage of lower resolution signal with higher samples in $\Delta \Sigma$ method simplifies the overall circuit complexity and therefore benefits cost efficiency. $\Delta \Sigma$ modulation converts the analog voltage into a pulse frequency output easily brought to time domain. This coarsely quantized output has found increasing usage in time domain signal processing. In time domain signal processing, variable is always measured and analyzed against time rather than its amplitude. Functions such as electronic signals, market behaviors are some example of time domain values. Time domain signal processing superiority, arguably is due to its lack of requirement for process such as filtering, amplifying and mixing plus its support for prediction and regression of the signal behavior over the time.

Further, time domain signal analysis makes it much easier to work in situation where the aim of analysis is to analyze and solve a time domain related problem; the SSCG in this dissertation is such one [19].

DTC converter is an algorithm to bring and convert digital signals (in voltage domain) to analog signal in time domain by component (period, width, phase) of the pulse according to the value. The process of converting signal from digital to analog usually involves many techniques such as filtering and smoothing of the signal before convention. DTC includes a digital $\Delta \Sigma$ modulator and samples are interpolated with analog low pass filter (LPF). In DTC, LPF is used to smooth the signal by cutting its high frequency components. Output signal is then converted to one-bit resolution timing signal.

DTC output signal spectrum can easily be manipulated by the algorithm and chosen parameters in the conversion process and its usage is found in spread spectrum clock generator and power circuits switching EMI removal [20].

Fig. 1.1 shows the circuit structure of spread spectrum clock generator. A sine wave
input to $\Delta \Sigma$ modulator, and a square wave with noise shaping is output through the $\Delta \Sigma$ modulator. Identification of this as a digital value of “0” on no modulation situation and “1” on modulation situation, and the digital value is input to the DTC. The clock signal is modulated according to the digital value that is $\Delta \Sigma$ modulated by the DTC, and the modulated clock signal is output.

![Diagram of spread spectrum clock generator](image)

**Figure 1.1 Circuit structure of spread spectrum clock generator**

Since the main cause of EMI is created by voltage, current switching synchronized with the circuit clock, in the noise spectrum, power is concentrated at a specific frequency (clock frequency and integral multiple frequency). It will lead to failure to meet EMI regulation. Fig.1.2 (a) shows the spectrum of pulse coding signal using fast Fourier transform (FFT). We can find that clock frequency does not meet EMI regulation. Here by modulating the clock signal using spread spectrum clock generator, the spread spectrum of pulse coding signal as shown in Fig. 1.2 (b). As a result, peak power is reduced and EMI problems can be reduced. However, as application in some signal bands (such as AM radio frequency $f_s$), it is not desirable to have noise from the spread clock. If spread spectrum using $\Delta \Sigma$ DTC algorithm implemented in programmatically configurable digital circuit, location of the required exclusion spectrum bands can be sensed and DTC algorithm parameters can change automatically (Fig. 1.2 (c)).
We introduce here that SSCG with proposed PWM ΔΣ DTC methods can adjust emission bands and excluding noise emission in specific bands.

First, Fig. 1.3 (a) shows the waveform without modulation (digital value = “0”). The parameter of the pulse wave is a rectangular wave with a period $T = 1ms$ (frequency: $f = 1kHz$), width $W = 200\mu s$, phase $\theta = 0$, duty ratio $D = 20\%$. Pulse Width Modulation (PWM) ΔΣ DTC changes the pulse width of the output signal based on the input digital value. As shown in Fig. 1.3 (b), when the digital value is “1”, the pulse width is set to $W_M$ (600\mu s in the figure). $W$ is the pulse width before modulation, $W_M$ is the pulse width after modulation, and let $W_M$ be smaller than one period. Fig. 1.4 shows an example of the generated pulse. It represents the pulse train when the ΔΣ modulated value “01011” is input. When $D = “0”$, no modulation is performed and $W = 200\mu s$, but when $D = “1”$, pulse width modulation is performed and $W_M = 600\mu s$ is modulated.
1.2.2 **Notch Frequency Generation due to Two-Coding Pulse**

Fig. 1.5 (a) shows the spectrum of the fundamental PWM (Fig. 1.3 (a)) using FFT. In the PWM method, when the pulse width is $W = 200 \mu s$ when input “0”, the period $T=1\text{ms}$, and $W_M = 600\mu s$ when input “1”. At this time, one notch appears shown in Fig. 1.5 (b) which equal to 2.5kHz. Then using a lot of simulations examined to find the notch frequency equation. The position of notch changes depending on the modulated value. When frequency $f=1\text{kHz}$ situation, set one square equal to $200\mu s$, the width before modulation is $W$, and after modulation is $W_M$. Notch can be created as following [21]:

$$f_{\text{notch}} = k \frac{(5\text{kHz} \times 200\mu s)}{(W_M - W)} = \frac{k}{400\mu s}$$  \hspace{1cm} (1.1)

where the notation $k$ denotes a positive integer. When $k = 1$, a notch is created at 2.5kHz which is the same as Fig. 1.5 (b). According to Eq. 1.1, the notch frequency is decided by only the difference of the pulse width. At here, predecessors developed an algorithm that uses $\Delta \Sigma$ modulation to spread the clock spectrum while allowing us to select the bands that we do not want to spread. We find that the notch characteristics can be applied in DC-DC switching converter to reduce EMI. Furthermore, the noise component of a specific frequency could be suppressed.
Figure 1.5 Spectrum of PWM using PWM ∆Σ DTC.

1.3 Organization of Dissertation

In this dissertation, we try to consider about some spread spectrum techniques for EMI reduction with suppressing diffusion of power supply noise and output ripple decrease. We discuss various kinds of DC-DC converter, and create methods in order to reduce EMI noise. Moreover, we propose a spread spectrum technique for clock pulse with suppressing diffusion of power supply noise using pulse width coding methods, based on the notch characteristics design. We expect that if notch frequency is set to the frequency of the received signal by adjusting the clock frequency. Therefore, just let the notch frequency be equal to the received signal frequency, and it will suppress noise in the received signal frequency and be not affected by other spread spectrum as we mentioned in section 1.2.

Chapter 1 introduces the background, the motivation and the objectives of this research. Chapter 2 discusses the basic topology and basic operation of DC-DC switching converter, and also discusses other types of switching power supply such as hysteretic control converter and soft switching converter and illustrates their merits and demerits. Chapter 3 presents proposes EMI reduction and creates output ripple decease method. Chapter 4 discusses notch frequency method with pulse coding control in DC-DC buck converter. Chapter 5 creates a full-automatic notch generation of pulse width coding switching converter. Chapter 6 confirms the notch frequency experimentally with the prototype circuit. Chapter 7 summarizes conclusions obtained through this research.
2. Conventional DC-DC Switching Converter

The DC-DC converter is the power converter of the switching power supply. Normally, a DC-DC converter is constituted by switching element (such as transistor and diode), inductor and capacitor. There are three available basic topologies according to the way of the inductor connection: buck converter (step-down type), boost converter (step-up type) and buck-boost converter (invert type). This chapter reviews their fundamental and also discusses other type of switching power supply such as hysteretic control converter and soft switching converter and illustrates their merits and demerits.

2.1 Basic Topology

DC-DC switching converter can be classified in terms of functions and operating methods, as shown in Fig. 2.1. A DC/DC switching converter can step down or step up the input voltage. As an extension of this capability, buck/boost conversion is also possible.

Pulse Width Modulation (PWM) and Pulse Frequency Modulation (PFM) are among the operation modes to control the output voltage. PWM provides regulation by adjusting the on/off time ratio at a constant switching cycle (frequency), whereas PFM uses a fixed on/off time ratio and a variable frequency. Also, a current mode, a voltage mode, and a hysteretic (or ripple, or comparator) control mode are among the available feedback control methods designed to regulate the output.

Switching converter is configured by a combination of these elements. The optimal combination must be selected based on the intended application, input/output conditions, design specifications and performance goals, cost, size and other restrictions to be met. The designer needs to know the characteristics as well as pros and cons of each element. We hope to design the low noise, high efficiency, low cost, compact, small ripple, low power consumption and fast response switching converter by combining various factors.
Fig. 2.2 shows the basic configuration of a DC-DC converter. A typical DC-DC switching converter includes a detection circuit, a reference voltage, an error amplification circuit, a PWM modulation circuit, a drive circuit, and a power stage. First, the DC input voltage is controlled by the power stage of the DC-DC converter. By this, it is converted into a high-frequency square wave. DC voltage output is obtained by smoothing this square wave. The output voltage is detected by the feedback circuit and compared with the reference voltage to amplify the error voltage. Then, according to the magnitude of the amplified error voltage, the PWM modulation circuit controls the on/off ratio of the switch through the drive circuit, thereby adjusting the output voltage so as to suppress the error voltage. This is the basic configuration of a DC-DC converter in a typical switching system.

There are three distinct rails possible for an inductor to be connected: the output, the input and the ground in DC-DC converter part. These three connecting ways realize three basic topologies of DC-DC switching converter. They are buck converter, boost converter and buck-boost converter respectively, as shown in Fig. 2.3.
Figure 2.2 Basic configuration of DC-DC switching converter.

Figure 2.3 Basic constitution of buck, boost, and buck-boost converters.

In the case of a PWM converter, the voltage applied to the switch and the waveform of the current flowing through the switch are approximately square waves, and Fig. 2.4 shows the operation of the switch SW, the current flowing through the switch $i_{sw}$, and the waveform of the voltage applied to the switch $V_{sw}$. Define the on-duty ratio $D$ and off-duty ratio $D'$ as Eq. 2.1 and 2.2. Here, $T_s$ is a switching cycle, $T_{on}$ is a switch-on period and $T_{off}$ is a switch-off period.
2.2 Basic Operation of DC-DC Switching Converter

2.2.1 Basic Operation of Buck Converter

Next, the operation of the most basic buck converter among DC-DC converters is explained. Figs. 2.5, 2.6, 2.7 show the basic circuit of a buck converter, and Fig. 2.8 shows its timing chart. This circuit contains a main power switch SW, a freewheeling diode D, an inductor L, an output capacitor C and a load resistor $R_L$. When the switch SW is on, the current is supplied from the input voltage $V_i$ to the output through the inductor $L$. At this time, the increase in the current $\Delta I_L$ flowing through the inductor is given by the following:

$$\Delta I_L = \frac{V_i - V_o}{L} \cdot T_{on}$$  \hspace{1cm} (2.3)

On the other hand, when SW is off, the current flowing in inductor $I_L$ is supplied to the load via $D$. At this time, the increase in the current $\Delta I_L$ flowing through the inductor is given by the following:
\[ \Delta I_L = -\frac{V_o}{L} \cdot T_{off} \quad (2.4) \]

In the steady-state, the amount of change in the inductor current during the on-period and the off-period is equal, so the following equation holds from (2.3) and (2.4).

\[ \frac{V_i - V_o}{L} \cdot T_{on} - \frac{V_o}{L} \cdot T_{off} = 0 \quad (2.5) \]

Rearranging Eq. 2.5, the following can be given:

\[ \frac{V_o}{V_i} = D \quad (2.6) \]

The above equation shows the relationship between the input/output voltage ratio and the duty ratio in the buck converter. From these relationships, it can be seen that the buck converter can control the output voltage by controlling the duty ratio.

![Basic circuit of buck converter.](image1)

![Buck converter when switch (SW) turns on.](image2)
The inductor current, the capacitor current and the output voltage is showing in Fig. 2.6. When the switch is on, the inductor current increases with the slope \((V_i - V_o)/L\). When the switch is off, the inductor current decreases with the slope \(V_o/L\). Since the voltage on the filter capacitor is equal to the output voltage, the voltage change across the capacitor is actually the ripple voltage of the output voltage.

![Diagram of Buck Converter](image)

Figure 2.7 Buck converter when switch (SW) turns off.

Fig. 2.8 shows a basic block diagram of the buck type DC-DC converter [23]-[24] with the Pulse Width Modulation (PWM) signal control and Fig. 2.9 shows its main signals. This converter consists of the power stage and the control stage. The power stage contains a main power switch SW, a freewheeling diode D, an inductor L, an output capacitor C and a load resistor R. The main switch is controlled by the PWM
signal from the control stage, which consists of an operational amplifier AMP, a comparator Comp and a reference voltage source $V_r$. First, when the PWM signal is high, the switch signal SW is turned on and the output voltage rises. Therefore, the error voltage $\Delta V$ is reduced and the duration of the PWM signal in high is shortened. To make the off-time of switch SW longer, the output voltage $V_o$ is going to decrease. As $V_o$ decreases, the error voltage $\Delta V$ increases. Therefore, the duration of the PWM signal at the low state is shortened. To make the on-time of the PWM signal SW longer, $V_o$ increases. By repeating this operation, $V_o$ is kept to be constant. The comparator Comp generates the PWM signal by comparing a saw-tooth signal SAW and the amplified error voltage $\Delta V$ as shown in Fig. 2.10. The saw-tooth generator resets and starts when the clock pulse rises.

![Figure 2.9 Voltage-mode negative feedback control circuit.](image)

![Figure 2.10 Waveforms in switching converter.](image)
2.2.2 Power Stage Transfer Function of Buck Converter

Since the DC-DC converter is a power circuit using negative feedback control, its stability is determined by the loop gain. However, it is not easy to derive the loop gain of DC-DC converter. Because the power stage of the DC-DC converter has two different operating states when the switch is on and off, the transfer function cannot be derived simply. Generally, the state-space averaging method [22] is used to derive the transfer function of the power stage in a DC-DC converter. So in the following, we will derive the transfer function of the power stage in the buck converter.

Fig. 2.11 shows the basic circuit of the power stage with equivalent resistance in the buck converter. This buck converter can be represented by the equivalent circuit by dividing it into an on-period and an off-period. Fig. 2.12 shows the equivalent circuit during the on-period, and Fig. 2.13 shows the equivalent circuit during the off-period. At here, \( r_s \) is the equivalent resistance of switch SW1, \( r_d \) is the equivalent series resistance of diode D, and \( r_L \) is the equivalent series resistance of inductor L. Here, the state equation is established on the assumption that the buck converter shown in Fig. 2.11 operates in the continuous current mode (CCM). Then we define state variables of inductor current \( i_L \) and capacitor voltage \( V_C \). Then, apply Kirchhoff's voltage law to the equivalent circuit of the on-period and the off-period, and derive the state equation in each period. In the following sections, we derive the state equation, the static and dynamic characteristics, and finally the transfer function of the converter.

![Figure 2.11 Basic circuit of power stage.](image)
First, let us derive the state equation. Deriving on-state equation according to Fig. 2.12 and applying Kirchhoff’s voltage law and current measurement to the inductor current $i_L$ and capacitor voltage $V_c$ gives the following equation:

\[
\frac{di_L}{dt} = -\frac{r_s + r_L}{L} i_L - \frac{1}{L} V_c + \frac{1}{L} V_i \\
\frac{dV_c}{dt} = \frac{1}{C} i_L - \frac{1}{CR} V_i
\]  

(2.7)  

(2.8)

Here, Eq. 2.7 and 2.8 using the state vector $X = \begin{bmatrix} i_L \\ V_c \end{bmatrix}$ can be expressed as the following:

\[
\frac{dX}{dt} = A_i X + B_i V_i
\]  

(2.9)
\[
\begin{bmatrix}
\frac{di_L}{dt} \\
\frac{dV_c}{dt}
\end{bmatrix} = \begin{bmatrix}
\frac{-r_s + r_d}{L} & -\frac{1}{L} \\
\frac{1}{C} & \frac{-1}{RC}
\end{bmatrix} \begin{bmatrix} i_L \\ V_c \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \end{bmatrix} V_i
\] (2.10)

Eq. 2.10 is the on-state equation in buck converter. Then using the same method can derive the off-state equation according Fig. 2.13.

\[
\frac{dX}{dt} = A_i X + B_i V_i
\] (2.11)

\[
\frac{di_L}{dt} = -\frac{r_s + r_d}{L} i_L - \frac{1}{L} V_c
\] (2.12)

\[
\frac{dV_c}{dt} = \frac{1}{C} i_L - \frac{1}{CR} V_i
\] (2.13)

So the off-state equation in the buck converter is like in the following Eq. 2.14.

\[
\begin{bmatrix}
\frac{di_L}{dt} \\
\frac{dV_c}{dt}
\end{bmatrix} = \begin{bmatrix}
\frac{-r_s + r_d}{L} & -\frac{1}{L} \\
\frac{1}{C} & \frac{-1}{RC}
\end{bmatrix} \begin{bmatrix} i_L \\ V_c \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} V_i
\] (2.14)

The weighted average of the state equation for the on-period and off-period at the duty ratio \(D\) becomes the following equation:

\[
\frac{dX}{dt} = (DA_1 + D A_2) X + (DB_1 + D B_2) V_i = AX + BV_i
\] (2.15)

Here, each coefficient matrix of Eq. 2.15 is:

\[
A = D \begin{bmatrix}
\frac{-r_s + r_d}{L} & \frac{-1}{L} \\
\frac{1}{C} & \frac{-1}{RC}
\end{bmatrix} + D' \begin{bmatrix}
\frac{-r_s + r_d}{L} & \frac{-1}{L} \\
\frac{1}{C} & \frac{-1}{RC}
\end{bmatrix} = \begin{bmatrix}
\frac{-r_s + r_d}{L} & \frac{-1}{L} \\
\frac{1}{C} & \frac{-1}{RC}
\end{bmatrix}
\] (2.16)

\[
B = D \begin{bmatrix}
\frac{1}{L} \\
0
\end{bmatrix} + D' \begin{bmatrix}
0 \\
0
\end{bmatrix} = \begin{bmatrix}
\frac{D}{L} \\
\frac{0}{0}
\end{bmatrix}
\] (2.17)

Here, \(r = r_L + D \cdot r_s + D' \cdot r_d\).

Then, let us show the static characteristics equation in the buck converter. In the static state, state variables and parameters do not change, as shown in the following equation:

\[
\frac{dX}{dt} = AX + BV_i = 0
\] (2.18)
According to Eq. 2.18, we can get $X = -A^{-1} \cdot B \cdot V_i$. So $X$ can be expressed as follows:

$$X = \frac{D / D V_i}{1 + Z_o / R} \left[ \frac{1}{D R} \right]$$

Here $Z_o$ is the internal resistance of the buck converter and is given by the following equation:

$$Z_o = D r_s + D r_D + r_L$$

Next, small signal dynamic characteristics is shown when the input voltage, duty ratio and load resistance are subjected to small deviations [22]-[25].

$$\begin{align*}
\Delta X &= \frac{1}{\Delta} \left[ \frac{s + \frac{1}{CR} - \frac{1}{L}}{1 + \frac{r}{L}} \right] \left[ \frac{r_L - r_s}{L} \right] X + \frac{1}{L} V_i \right] \left[ \frac{1}{L} \right] V_i \\
&= \frac{V_o}{P(s)} \left[ 1 + \frac{(r_L + r_s)}{R} \right] \left[ 1 \right]
\end{align*}$$

Using the same method, Eq. 2.25 is a transfer function that indicates the change in output voltage $V_o$ with respect to the change in input voltage $V_i$.

$$\begin{align*}
\frac{\Delta V_o}{\Delta D} &= \frac{V_o}{P(s)} \frac{1 + (r_L + r_s)}{R} = \frac{G_{vib}}{P(s)}
\end{align*}$$

Eq. 2.26 is a transfer function that indicates the change in output voltage $V_o$ with
respect to the change in resistance $R$.

$$\frac{\Delta V_o}{\Delta R} = \frac{V_o}{P(s)} \frac{Z_o / R^2}{(1 + s \cdot L / Z_o)} \cdot (1 + s \cdot L / Z_o) = \frac{G_m(s)}{P(s)} (1 + s / \sigma_r)$$ (2.26)

In the case of a switching power supply, the duty ratio $D$, the load resistance $R$, and the input voltage $V_i$ are considered as external parameters, and Fig. 2.14 shows a block diagram of the buck converter. The error voltage amplifier and PWM converter in the control circuit are linear conversions and can be replaced by a constant $K$. Here, the transfer function of the phase compensation circuit performed by the error amplifier is not described. At this time, the loop transfer function $G_o(s)$ is basically a quadratic equation, in an actual circuit, a phase delay occurs due to a delay caused by discrete control of an amplifier and a PWM signal, and the power supply system tends to be unstable. In Fig. 2.14, the load current fluctuation is equivalently indicated by load resistance change $\Delta R$ and input voltage change is indicated by $\Delta V_i$. The block after the power supply $P(s)$ represents the effect of the output impedance $Z_o$ on the actual power supply.

Figure 2.14 CCM block diagram of buck converter.

At last, the characteristics of the buck converter is analyzed with the simulation software SIMPLIS. The parameters used there are shown in Table 2.1 and the loop transfer function is shown in Fig. 2.15 using a Bode diagram. Here, the internal resistance of the switch and inductor are $50 \text{m} \Omega$ and $10 \text{m} \Omega$, the ESR of the capacitor is $220 \text{m} \Omega$, and the GB product of the operational amplifier is $100 \text{ MHz}$. From Fig. 2.15 we can found that the phase margin is about $50$ degrees. The gain changes at the frequency where the phase becomes $90$ degrees, and we can find that the resonance phenomenon occurs at $1.50 \text{kHz}$. According to the transfer function, the resonance
frequency \( f = \frac{1}{2\pi \sqrt{LC}} = \frac{1}{2\pi \sqrt{50 \times 10^{-6} \times 220 \times 10^{-6}}} = 1.52 kHz \) is obtained, which roughly equal to the value on the Fig 2.15.

<table>
<thead>
<tr>
<th>Parameters of the buck converter.</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_i )</td>
</tr>
<tr>
<td>10V</td>
</tr>
<tr>
<td>( L )</td>
</tr>
<tr>
<td>50( \mu )H</td>
</tr>
</tbody>
</table>

Figure 2.15 Bode diagram of the buck converter.

2.2.3 Boost Converter

In the following, the operation of the boost converter is explained. Figs. 2.16, 2.17, 2.18 shows the basic circuit of the boost converter, and Fig. 2.19 shows the timing chart of the boost converter under steady state. Similar to the buck converter in previous section, the switch can be set at two positions alternately, and the circuit operates at on-state and off-state accordingly, as shown in Fig. 2.17 and Fig. 2.18.

When the switch SW is on, the energy storage in coil and the inductor current increases by the slope \( V_i/L \). When switch SW is off, the inductor current decreases by the slope \((V_o - V_i)/L\).

When the switch SW is on, the increase in the current \( \Delta I_L \) flowing through the inductor is given by following:

\[
\Delta I_L = \frac{V_i}{L} \cdot T_{on} \tag{2.27}
\]

On the other hand, when SW is off, supply energy to the load via D from power supply
$E$ and coil $L$. At this time, the increase in the current $\Delta I_L$ flowing through the inductor is given by following:

$$\Delta I_L = -\frac{V_o - V_i}{L} T_{off}$$

(2.28)

According to the steady-state principle of the inductor volt-second balance, the relation between the input voltage and the output voltage is obtained

$$\frac{V_i \cdot T_{on}}{L} - \frac{(V_o - V_i) \cdot T_{off}}{L} = 0$$

(2.29)

Rearranging Eq. 2.29, the following can be given:

$$\frac{V_o}{V_i} = \frac{T_{on}}{T_{off}} = \frac{1}{D}$$

(2.30)

The above equation shows the relationship between the input/output voltage ratio and the duty ratio in the boost converter. From these relationships, it can be seen that the output voltage $V_o$ of the boost converter must be larger than the input voltage $V_i$.

![Basic circuit of the boost converter.](image1)

![Boost converter when switch (SW) turns on.](image2)
2.2.4 Buck-boost converter

The converters in Figs. 2.20, 2.21 and 2.22 are boost converter. When the switch SW is on, the inductor current increases by the slope \( V_i/L \). When the switch SW is off, the inductor current decreases by the slope \( V_o/L \). The timing chart of the buck-boost converter under steady state is as shown in Fig. 2.23.

When the switch SW is on, the increase in the current \( \Delta I_L \) flowing through the
inductor is given by the following:

\[ \Delta I_L = \frac{V}{L} \cdot T_{on} \]  
\[(2.31)\]

On the other hand, when SW is off, the increase in the current \( \Delta I_L \) flowing through the inductor is given by the following:

\[ \Delta I_L = -\frac{V_o}{L} \cdot T_{off} \] 
\[(2.32)\]

In the steady-state, the amount of change in the inductor current during the on-period and the off-period is equal, so the following equation holds:

\[ \frac{V}{L} \cdot T_{on} - \frac{V_o}{L} \cdot T_{off} = 0 \] 
\[(2.33)\]

Rearranging Eq. 2.33, the following can be given:

\[ \frac{V_o}{V_i} = \frac{T_{on}}{T_{off}} = \frac{D}{D} \] 
\[(2.34)\]

From Eq. 2.34, we can know that the output of buck-boost converter is an inverting voltage. When \( 0 \leq D < 0.5 \), the output voltage is reduced. When \( 0.5 < D \leq 1 \), the output voltage is amplified. Also when \( D = 0.5 \), we can get \( V_o = -V_i \).

![Figure 2.20 Basic circuit of the buck-boost converter.](image-url)
Figure 2.21 Buck-boost converter when switch (S) turns on.

Figure 2.22 Buck-boost converter when switch (S) turns off.
2.3 Hysteretic Control Switching Converter

Roughly, there are two control methods for stabilizing the operation of the DC-DC converter; linear control and nonlinear control. Linear control is such as voltage mode control and current mode control. The output voltage is stabilized by adjusting the timing at which the switching element is turned on and off using a fixed-frequency PWM (pulse width modulation) signal, which is used in a very wide range of fields from portable electronic devices to industrial electronic devices. That is, it can be applied to both low power output and high power output. However, it has the disadvantage that the response speed to sudden changes in load is relatively slow. Its reasons are delay due to the frequency characteristics of the error amplifier in the feedback loop, dead time delay equivalent to one cycle of the switching operation, and delay due to the frequency characteristic of the phase compensation circuit including the LC filter. Nonlinear control such as hysteretic controlled has the advantage of high response speed to sudden load changes and it can be realized with a simple circuit configuration.
2.3.1 Basic Operation of Hysteretic Control Converter

The hysteresis control method was developed to meet the power requirements of even faster load transient response of load elements, such as CPU and FPGA. Because it performs controls by detecting ripples in the output, this method is also referred to as a ripple control method. The method directly monitors the output voltage by means of a hysteresis comparator without going through an error amplifier. When detecting that the output voltage has exceeded or fallen below a set threshold level, the comparator directly turns the switch on/off. The three control schemes are available: hysteresis window method, bottom detection on-time fixed method and upper detection off-time method. The hysteresis window method is using the thresholds provided on the upper side and the bottom side, that is, using the hysteresis window to control the timing of turning on/off the switching element. Bottom detection on-time fixed method is detecting a voltage below the threshold level with a fixed on-time. Upper detection off-time fixed method is detecting above the threshold with a fixed off-time. Fig. 2.24 shows the diagram and Fig. 2.25 shows the operation waveforms of the hysteretic control buck converter.

![Figure 2.24 Basic hysteretic control buck converter.](image-url)
The basic operation of the hysteretic control method is explained as the following. The comparator is a hysteresis comparator, which has a slight hysteresis to prevent chattering and to limit the operating frequency. When the switch SW turns off, the output voltage $V_o$ decreases. When the output voltage $V_o$ falls below the reference voltage $V_{ref}$ of the non-inverting terminal, the PWM signal output from hysteretic-comparator becomes high with a short delay, and SW turns ON. As a result, $V_o$ increases. When $V_o$ exceeds $V_{ref}$, after a short delay, the PWM signal goes low and SW turns OFF. As a result, $V_o$ decreases again. By repeating the above operation, control is performed so that $V_o$ matches a constant voltage $V_{ref}$. The operating time $T_{op}$ is determined by the next equation:

$$T_{op} = 2 \cdot (t_{sw} + t_{il} + t_C + t_{comp})$$

(2.35)

Here, $t_{sw}$ means the delay of SW, $t_C$ means the integrated time by C and $t_{comp}$ means the delay of the comparator. Usually this delay time $t_{op}$ is less than 1$\mu$s.

### 2.3.2 Features of Hysteretic Control Converter

This control method does not use an error amplifier. Instead, it uses a comparator. The comparator compares the output voltage with the reference voltage to control the on/off timing of the switching element. Therefore, there is no delay due to the frequency characteristics of the error amplifier and no dead time delay of one cycle of the switching operation. It is the inductance component of the LC filter that determines the response speed. Therefore, a very high response speed can be obtained even if the switching frequency is low. Simultaneously, since the control system can be configured with only the comparator, the system is essentially stable. Therefore, there is no need to design a compensation circuit.
On the other hand, the hysteretic control method also has disadvantages as follows:

1) Since the comparator is driven by using the ripple component of the output voltage, there is a disadvantage that an output capacitor having a relatively large equivalent series resistance (ESR) is required, and hence large output voltage ripple occurs.

2) The fast operation with switching the voltage and the current generates the large EMI noise, which emits the unnecessary noise to the air and the conductive noise in the input power line.

3) Since it is clock-less control and the switching frequency fluctuates depending on the load conditions, clock frequency modulation is difficult and EMI countermeasures using the conventional method were difficult.

Recently, control methods have been introduced that solve these disadvantages. Specifically, there are a Constant On Time (COT) method and a ripple injection method. If the former is used, fluctuations in the switching frequency can be minimized and EMI measures can be simplified. The latter allows the use of low ESR multilayer ceramic capacitors as output capacitors. This makes it possible to reduce the size of the power supply circuit.

2.3.3 COT Type Hysteretic Control Converter

The COT control method is one of the control methods of a feedback circuit that stabilizes the output voltage in a DC-DC converter. Broadly classified, it is included in the hysteretic control method.

The biggest feature of COT type hysteretic control is that it can achieve high-speed load response characteristics. Microprocessors, DSPs, FPGAs, ASICs, etc., have changed their operation modes in order to reduce power consumption. For example, switching from full operation mode to low power consumption mode, or switching from standby mode to full operation mode, at the time of such mode switching, a current supplied to a microprocessor, a DSP, an FPGA, an ASIC, that is called load current greatly changes. At that time, the output voltage also fluctuates greatly, and in some cases, the output voltage is out of the allowable range, and the microprocessor or the like may malfunction. If using the COT control method, it can minimize fluctuations in the output voltage, so that malfunctions of microprocessors also can be prevented.

In the COT control method (Fig. 2.26), only the lower threshold of the output voltage is set (Fig. 2.27) and there is no upper threshold. Instead, the on-time is fixed.
Specifically, when the output voltage reaches the lower threshold, the switching element is turned on. Then, the switching element is automatically turned off when a predetermined on time elapses. Like this operation, the output voltage is stabilized.

![COT type hysteretic control buck converter](image1)

Figure 2.26 COT type hysteretic control buck converter.

![Timing chart of COT type hysteretic control buck converter](image2)

Figure 2.27 Timing chart of COT type hysteretic control buck converter.

With this method, the on-time is constant, so the operating frequency is constant in the steady state regardless of the magnitude of the load current. But the operating frequency is changed on Discontinuous Conduction Mode (DCM) or for the change of the input voltage $V_i$. 

29
2.3.4 Ripple Injection Method of Hysteretic Control Converter

Fig. 2.28 shows the circuit of the ripple injection method of the hysteretic control converter, and Fig. 2.29 shows the waveform of this converter. In order to generate the large ripple (or the triangular signal) synchronized with the output voltage ripple $\Delta V_o$ or the PWM pulse, the $C_f R_f$ circuit is added across the inductor. This large ripple is injected into the ripple $\Delta V_i$, which is much larger than $\Delta V_o$ and connected to the negative input of the comparator through the coupling capacitor $C_b$. The PWM pulse is easily generated to compare this large signal with the reference voltage $V_r$. There is no need to use the hysteresis comparator nor the high ESR capacitor. No need of hysteresis comparator keeps the high frequency response and using the low ESR of the capacitor makes the output ripple very small [27].

Figure 2.28 Ripple injection method buck converter.
2.4 Soft Switching Converter

The development trend of modern power electronic devices is miniaturization and weight reduction, and at the same time, higher requirements for device efficiency and electromagnetic compatibility. Generally, filter inductors, capacitors, and transformers account for a large proportion of the size and weight of a device. We know that increasing the switching frequency can reduce the parameters of the filter and miniaturize the transformer; thereby they effectively reduce the size and weight of the device. Therefore, the most direct way to reduce the size and weight of the device is to increase the frequency of the circuit. However, as the switching frequency is increased, the switching loss also increases, the circuit efficiency is severely reduced, and the electromagnetic interference is also increased; so simply increasing the switching frequency is not feasible. In order to deal with these problems, soft switching technology has appeared, which mainly solves the switching loss and switching noise problems in the circuit, and the switching frequency can be greatly increased.

2.4.1 Features of Soft Switching Converter

As shown in Fig. 2.4 in Section 2.1, in this circuit, the voltage and current are not zero during the switching process, and there is overlap, so there is a significant switching loss. The speed of voltage and current changes is very fast, and the waveform has obvious overshoot, which results in switching noise. This switching process is called hard switching. The switching loss has a linear relationship with the switching
frequency, so when the operating frequency of the hard circuit is not too high, the switching loss accounts for a small proportion of the total loss. However, as the switching frequency increases, switching losses become more and more significant. This time, soft switching technology must be used to reduce switching losses.

A typical soft switching circuit is a buck type Zero Voltage Switching (ZVS) resonant circuit. The voltage and current waveforms during the switching process are shown in Fig. 2.31. Compared with the hard switching circuit voltage and current waveforms (Fig. 2.30), low switching losses created during switch off and on process.

Figure 2.30 Voltage and current during hard switching (a): off-process (b): on-process.

Figure 2.31 Voltage and current during soft switching (a): off-process (b): on-process.
2.4.2 Basic Operation of Soft Switching Converter

Compared with the hard switching circuit, the resonant inductance $L_r$ and the resonant capacitance $C_r$ are added to the soft switching circuit shown in Fig. 2.32. Compared to filter inductors and capacitors, the values of $L_r$ and $C_r$ are much smaller. After the switch is turned off, resonance occurs between $L_r$ and $C_r$, and the waveform of voltage and current in the circuit is similar to a sine half wave. Resonance slows down the changes in voltage and current during switching, and reduces the voltage across the switch to zero before it turns on. This significantly reduces switching losses and switching noise.

Before the switch is turned on, the voltage across it is zero. When the switch is turned on, there will be no loss and noise. This turn-on method is called zero voltage switching operation. Before the switch is turned off, its current is zero, and no loss and noise will be generated when the switch is turned off. This shutdown method is called zero current switching operation. Next, let us introduce about basic operation of the voltage-mode resonant switching converter with ZVS operation.

Fig. 2.32 shows the circuit of the full-wave type voltage-mode resonant converter. This converter contains a main power switch $SW$, a free-wheel diode $D_0$, a main inductor $L_o$, an output capacitor $C_o$ and resonant elements which are an inductor $L_r$, a capacitor $C_r$ and a diode $D_r$; if there is no $D_r$, it will form a half-wave type soft-switching converter.

The operation of the full-wave resonant converter can be divided into the following 6 states in one switching period, and Fig. 2.33 shows its major signal waveforms [28]:

**State 0:** $T_0 < t < T_1$: Before the time $T_0$, the switch keeps on and $D_0$ keeps off, $u_{Cr} = 0$, $i_{Lr} = I_L$; when $t = T_0$, the switch is turned off, the capacitor $C_r$ is charged with current and the capacitor voltage $u_r$ rises linearly from zero. At the same time, the voltage of the diode $V_d$ drops. Until $t = T_1$, $V_d = 0$, the diode is turned on.

**State 1:** $T_1 < t < T_2$: When $t = T_1$, the diode is turned on. $C_r$ resonates with the $L_r$. In resonance period, $L_r$ charges $C_r$, and $u_{Cr}$ continues to rise, while $i_{Lr}$ continues to fall, until $t = T_2$, $i_{Lr}$ drops to zero, and $u_r$ reaches the resonance peak.

**State 2:** $T_2 < t < T_3$: When $t = T_2$, $C_r$ discharges to $L_r$, current changes direction, $u_{Cr}$ keeps going down until $t = T_3$, $u_{Cr} = V_{in}$. At this time, the voltage across $L_r$ is 0 and $i_{Lr}$ reaches the peak reverse resonance.

**State 3:** $T_3 < t < T_4$: The $L_r$ reverse charging the $C_r$, the $u_{Cr}$ continues to drop, until $t = T_4$, $u_{Cr} = 0$. 

33
**State 4:** $T_4 < t < T_5$: $u_{Cr}$ resonates in the negative direction after $u_{Cr} = 0$. The switch is turned on during this time. When $u_{Cr}$ becomes zero again, the resonance state ends and enters to next state.

**State 5:** $T_5 < t < T_6$: $i_{Lr}$ rises linearly, until $t = T_6$, $V_d$ turns off. During this period, $u_{in}$ drops to the $D_o$ and $i_{Lr}$ flows through the switch. This state continues until the next turn off operation.

Here, when switch is on, the voltage across it is 0V, and ZVS is realized. Further, when the switch is off, the voltage across it is 0V and it is maintained by $C_r$, which is also the ZVS operation.

![Figure 2.32 Full-wave resonant soft-switching.](image)

![Figure 2.33 Timing chart of full-wave resonant soft-switching.](image)
Using resonance to realize the ZVS operation, a soft-switching converter can realize high efficiency and low EMI noise. However, unnecessary radiation and conduction noises of the input current by the switch are still large. This kind of converter has an operating frequency dependent on the resonant waveform. Since the fixed frequency clock is not used, the frequency modulation of the PWM operation signal is strict and the EMI reduction is difficult.

2.5 Summary

This chapter reviews the basic structure and operating principle of buck converter, boost converter, buck-boost converter, hysteretic control switching converter and soft switching converter, and then discusses their merits and demerits.

The merits of buck, boost and buck-boost converter are high efficiency, low cost and compact. On the other hand, their switching noise is inevitable. This noise generation is a major disadvantage of the DC-DC converter. The hysteretic control switching converter does not have a concept of a loop response, and is operated by a comparator (comparing circuit), so that its response is fast. Moreover, since a compensator is not required, the design is simple, and it has been widely used as a power supply for electronic devices that require a high-speed response. On the other hand, there are some demerits such as large output voltage ripple, substantial EMI noise. Soft switching has the great advantage of suppressing switching loss and harmonic noise. On the other hand, since soft switching is realized using the $L$ and $C$ resonance phenomena, conduction loss is increased due to resonance current.

In the next chapter, we will propose new EMI reduction technologies with buck converter, hysteretic control switching converter and soft switching converter.
3. EMI Noise Reduction Technology

EMI stands for Electromagnetic Interference. We usually refer to any unintentional power transfer between a source and a victim. Types of EMI are conducted emission and radiated emission. Conductive emission is propagated through wires and PCB wiring. Radiated emission is a type of noise that is emitted (radiated) through the air.

EMI has always been an issue in electrical devices. In the early years of (analog) electronics the main concern was the generation of disturbances in the victim. For example, analog TV systems have been developed with a 50 Hz or 60 Hz frame-rate in order to minimize the flickering effect due to interference coming from nearby 50/60 Hz AC devices [29].

In recent years, the communication circuit has been accelerated to be powerful and to have higher density packaging. The fluctuation of the switching noise has strongly spread in the wide frequency range with the acceleration of high-speed and high-frequency electronic equipment. EMI-related problems have received considerable attention, as proven by the presence of many international regulations [30], aiming to impose/guarantee the electromagnetic compatibility (EMC) of any electronic device. That is, any electronic equipment must not generate EMI above a tolerable level, and must be not susceptible to EMI if it is below a tolerable level.

In order to reduce the switching noise of high-speed and high-frequency electronic equipment, complex noise filtering and shielding are needed [5], which makes the switching power supply larger in size and costly. There were some techniques for broadening and flattening their switching noise power spectrum to reduce EMI such as a spread spectrum method that randomly modulates the clock signal [6]-[9] or chaos-based pulse width modulation [12]-[17]. Frequency modulation techniques have been used to reduce EMI noise by modulating the original constant clock frequency in order to spread the energy of each single harmonic into a certain frequency band, thus reducing the peak amplitude of EMI at harmonic frequencies. Frequency modulation such as frequency hopping modulation, digital phase modulation, linear sweep frequency modulation and analog random frequency modulation are often used.

In the frequency hopping technique, for the simple case of only two hopping frequencies, the resulting spectrum of $V_{SW}$ can be predicted using Fig. 3.1, where $V_{SW}$ is viewed as the sum of two components. Each component is modeled as the result of the random digital sequences $P_1$ and $P_2$ modulating carrier signals $V_{C1}$ and $V_{C2}$,
respectively. The result of this modulation is that the spectrum of the random digital sequences $P_1$ and $P_2$ gets upconverted to $f_1$ and $f_2$, respectively. The spectrum of the random digital sequences $P_1$ and $P_2$ contains dc energy (a spur at dc), as well as spread-out energy (modeled as a sinc function [31]) due to the randomness of the sequence. Therefore, two spurs at $f_1$ and $f_2$ appear in the spectrum of $V_{SW}$ with slightly elevated random noise floor. While applying frequency hopping to buck converters can reduce output spurs, there are implementation difficulties that must be addressed. Changing the switching frequency disturbs the steady-state switching duty cycle of the converter if the hopping instant occurs at the middle of a ramp cycle. In this case, resetting the ramp in order to start a new ramp cycle at a different frequency can cause pulse swallowing or significant instantaneous error in the duty cycle. This duty cycle disturbance manifests itself in the form of transients or glitches at the output of the converter every time hopping occurs, which interferes with the operation of the load [32].

![Waveforms analysis of a frequency-hopped buck converter with two hopping frequencies.](image)

In the digital phase modulation, basic clock sequentially stored in shift register. Select by random signal for each cycle, random phase clock can be created. The demerits of digital phase modulation method are large size and need many components. For example when phase shift circuit is about 10~12bit situation, 1000~4000 shift registers and selectors are needed [9].

In this chapter, we propose new EMI reduction technologies and automatic output voltage ripple cancellation method for the PWM buck converter with voltage-mode, the hysteretic controlled switching converter and the soft switching converter. Normally, modifying the clock frequency is effective to reduce the EMI noise, but it may increase the output ripple. We also have developed techniques to cancel the increased ripple by modifying the slope of the saw-tooth signal or current of the ripple injection circuit.
3.1 EMI Reduction with PWM Control Converter

In an electronic device, radiation at a clock frequency and harmonics of a clock used in a digital processor or a power supply circuit is increased, which affects other electronic devices such as malfunction. Similarly, switching noise of high voltage and large current becomes radiation noise and interferes with the surroundings. For this reason, EMI regulations are stipulated in many countries. For example, Fig. 3.2 shows the information of CISPR (International Special Committee on Radio Interference) 22 indicates noise regulations in radiation noise for information technology equipment. The dark and light lines indicate the upper limit of EMI for commercial · light industry and home use, respectively. Exceeding this limit will affect other electronic devices. There are some techniques to meet this limit, such as using shielding or filtering. The use of shielding increases the overall cost while the use of filtering increases the size. As we mentioned early, one of the methods for reducing such electromagnetic radiation is a spread spectrum clock generation technique. This technology can significantly reduce EMI and since the generation of noise is suppressed by the "source", there is an advantage that the number of parts for general noise suppression can be greatly reduced.

Figure 3.2 EMI regulation in radiation noise (CISPR22) in Japan.

3.1.1 Conventional EMI Noise with PWM Control Buck Converter

Type of EMI are conducted noise and radiated noise. The EMI (especially the peak of radiated noise) generated by switching is mainly caused by the resonance of stray L, C components existing on the switching itself and its peripheral circuits. It is possible to suppress the noise generated in the resonance loop that uses the voltage applied to the device [33]-[34]. The EMI noise reduction we are studying is the conduction noise which returns to the input of the power supply, and we are not considering the radiation
noise here. Therefore, in conjunction with reducing the low frequency noise of the PWM pulse, the PWM frequency and its harmonic noise are reduced and the conduction noise is proportionally attenuated.

The basic action of the buck converter with PWM control method is explained in part 2.2.1, and Fig. 3.3 shows its circuit diagram. The parameters of this buck converter are shown in Table 3.1. Here, as the switching signal of high power is increased in speed, large noise is generated. Fig. 3.4 shows the spectrum of the PWM signal in the buck converter (Fig. 3.3). There is the line spectrum at the frequency of the clock (0.5MHz) which is equal to 3.5V and there appear many harmonic spectra.

![Buck converter with PWM signal control](image)

**Figure 3.3** Buck converter with PWM signal control.

![Simulated spectrum without EMI reduction](image)

**Figure 3.4** Simulated spectrum without EMI reduction.
Table 3.1 Parameter values of simulation circuit.

<table>
<thead>
<tr>
<th>$V_i$</th>
<th>$V_o$</th>
<th>$I_o$</th>
</tr>
</thead>
<tbody>
<tr>
<td>12V</td>
<td>5V</td>
<td>0.25A</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>$L$</th>
<th>$C$</th>
<th>$T_{ck}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>200μH</td>
<td>470μF</td>
<td>2.0μs</td>
</tr>
</tbody>
</table>

3.1.2 EMI Noise Reduction with Clock Frequency Modulation

In order to reduce the clock noise, the clock pulse modulation is used by shaking the frequency of the saw-tooth generator (Fig. 3.5). This circuit consists of the saw-tooth SAW generator, the Voltage Controlled Oscillator (VCO) and the control voltage signal. The output frequency $F_{ck}$ of the VCO is represented by Eq. 3.1. The control voltage $V_{con}$ is set to the base DC voltage $V_b$=4.0V and the modulation signal, which is the triangular signal set to the frequency $F_m$=1kHz and the amplitude $V_m$=±1.0V. $K$ is the sensibility of the VCO ($K$=50[kHz/V]). The frequency of the VCO output is modulated from 150kHz to 250kHz.

$$F_{ck} = K \cdot V_{con} = K \cdot (V_b + V_m)$$  \hspace{1cm} (3.1)

Fig. 3.6 shows the modulated spectra of the PWM pulse. The $F_{ck}$ peak level of the PWM pulse is from 3.5V to 673mV, which is about 14 dB reduction. There is no line spectrum in harmonic frequencies. With this modulation, the output ripple becomes very large from 3 m$V_{pp}$ to 18 m$V_{pp}$ according to Fig. 3.7. This large ripple is no good for the voltage regulators and it should be improved.
3.1.3 EMI Reduction & Output Ripple Improvement

With the frequency modulation, the duty $D$ of the PWM pulse is also modulated and the output voltage is a little up and down shown in Fig. 3.7. To improve this modulated ripple, we have developed the cancellation method by correcting the duty change of the PWM pulse, as shown in Fig. 3.8. Assume that the modulation signal is becoming higher and the clock frequency is modulated to be higher and the period of the SAW signal is becoming smaller. In this case, the slope of the SAW signal is not changed and
the output pulse width of the comparator is also not changed. Then the duty $D$ of the PWM pulse is a little increased. To correct this duty increase, the slope of the SAW signal is linearly increased with the modulation signal $V_m$ shown in Fig. 3.9. In this case, the peak voltages of the original SAW signal and of the corrected SAW signal are the same values [35].

To design the conductance value $g_m$ in the correction circuit of Fig. 3.8, we need to analyze the optimum conductance $g_m$. First, assuming that the conversion rate (sensitivity) of the VCO is $K$ (kHz/V), the modulation signal base voltage is $V_b$, the modulation signal amplitude is $V_m$, and the modulation rate $\alpha = V_m/V_b$. Here, the clock frequency after modulation $F_{ck}'$ is given by the following Eq. 3.2.

$$F_{ck}' = K \cdot (V_b \pm V_m) = KV_b(1 \pm \frac{V_m}{V_b}) = KV_b(1 \pm \alpha)$$  \hspace{1cm} (3.2)

For example, when the modulation rate $\alpha = 0.1$, the modulated clock frequency $F_{ck}'$ is a frequency modulated by $\pm$ 10% compared to the original clock frequency $F_{ck}$. Here, similarly to the modulation part, by correcting the current of $\alpha$, the slope of the saw-tooth wave is corrected, and the change of duty can also be suppressed. Normally, the saw-tooth wave correction current $dI_{SAW}$ can be expressed as in Eq. 3.3, assuming that this is the same value as $\alpha I_{SAW}$ for which the current has been corrected by $\alpha$, the optimum current correction amount $g_m$ can be derived as shown in the following equation Eq. 3.4.

$$dI_{SAW} = g_m \cdot V_m$$  \hspace{1cm} (3.3)

$$dI_{SAW} = \alpha I_{SAW}$$

$$g_m \cdot V_m = \frac{V_m}{V_b} I_{SAW}$$

$$g_m = \frac{I_{SAW}}{V_b}$$  \hspace{1cm} (3.4)

Simulation was performed by adding the correction circuit in Fig. 3.8 to the one in Fig. 3.5. Simulation parameters are in Table 3.2. The conditions of the correction circuit section are as follows: saw-tooth wave generation current source $I_{SAW} = 1.0mA$, current correction amount $g_m = 200 \sim 300\mu S$ (S: Siemens, a unit of electrical conductance). Further, when $I_{SAW} = 1.0mA$ and the modulation signal base voltage $V_b = 4V$ and is substituted into Eq. 3.4, the theoretical value of the current correction amount in this simulation circuit is $g_m = 250\mu S$. 

42
Fig. 3.10 shows the original ripple $V_o$, modulated ripple $V_{om}$ and corrected ripple $V_{oc}$, respectively. The correct ripple is almost the same as the original non-modulated ripple.
It is well-known that EMI noise is very serious problem which occurs from switching the input voltage and the large current. We adopt the PWM noise as the EMI noise and investigate the conductive noise which is the input current noise in the input power line. In order to reduce the EMI noise, it is usually used to modify the clock frequency or phase. For the clock-less hysteretic control converter, it is difficult to shake the PWM pulse. We have modified the width of the COT pulse to shake the frequency of the operating pulse to reduce EMI noise, and created the method to cancel the output voltage ripple.

### 3.2.1 Conventional Hysteretic Control Converter using COT Method

For the basic hysteretic control converter, the operation frequency $F_{op}$ is variable, depending on the load current $I_o$, which affects the characteristics of the loop transfer function. In order to make $F_{op}$ stable against $I_o$, it is agreeable to set the on-time $T_{on}$ (or off-time) constant because the operation period is decided by the relationship
between the duty ratio $D$ and the on-time of the PWM pulse. When $T_{ON}$ is set, $T_{OP}$ is automatically controlled as the next equation. Eq. 3.5.

$$T_{op} = \frac{1}{F_{op}} = \frac{T_{on}}{D} \frac{T_{on}}{V_i} \frac{V_i}{V_o}$$

(3.5)

From this equation, we can find change load resistance will not affect the output voltage. When the load current is half of the peak-to-peak value of the ramp of $I_L$, the lowest point of the ramp drops to zero (Fig. 3.12). At this lowest point, the inductor current is zero and the energy storage is zero. If the load current is further reduced, the inductor will enter a discontinuous current mode (DCM). In this situation, the output voltage and on-time $T_{on}$ is constant, but the operating frequency changes low. Fig. 3.11 shows the configuration of the buck converter using the COT control method, and Fig. 3.12 shows its operating waveforms. The COT pulse is generated at the positive edge of the output pulse of the comparator. Simulation parameters are in Table 3.3. The waveform of the COT pulse generator is shown in red border (Fig. 3.11). It consists of a saw-tooth SAW generator, a comparator Comp2 and the COT reference voltage $V_{rCOT}$. The SAW generator includes a switch, a current source $I_{COT}$ and a capacitor $C_{COT}$. The switch is controlled by the positive edge of $V_{comp}$ and resets / starts the SAW signal. The COT pulse is generated by comparing the SAW signal with the COT voltage reference $V_{rCOT}$, and $T_{COT}$ is calculated with the next equation Eq. 3.6.

$$T_{COT} = \frac{V_{rCOT} \cdot C_{COT}}{I_{c}}$$

(3.6)

<table>
<thead>
<tr>
<th>$V_i$</th>
<th>$V_o$</th>
<th>$L$</th>
</tr>
</thead>
<tbody>
<tr>
<td>10V</td>
<td>3V</td>
<td>10μH</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>$C$</th>
<th>$V_{rCOT}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>10μF</td>
<td>0.51V</td>
</tr>
</tbody>
</table>
3.2.2 EMI Noise Reduction with COT Control Method

For the clock-less control converter, it is difficult to shake the PWM pulse. We have modified the width of the COT pulse to reduce the peak level of the PWM frequency in the spread spectrum.
Fig. 3.13 shows the block diagram of the COT converter with EMI noise reduction. In Fig. 3.13, the reference voltage \( V_{rcot} \) is modified by the triangular signal and the variation of \( V_{rcot} \) modifies the COT pulse width \( T_{cot} \) shown in Fig. 3.14. The frequency of the modified signal is \( F_m = 1.0 \text{ kHz} \) and \( V_{rcot} \) is 2.4VDC + 0.25Vpp AC.

![Block Diagram](image1)

Figure 3.13 EMI noise reduction with COT control circuit.

![Timing Chart](image2)

Figure 3.14 Timing chart of modified COT pulse.

Fig. 3.15 shows the COT control method spectrum without EMI reduction, in which
the red spectrum is the PWM noise and the green one is the conductive noise. The peak level of the PWM frequency ($f = 940$ kHz) is 2.7 V and that of the conductive noise is 1.0V, which is -8.6 dB of that of the PWM spectrum. The spectrums of the harmonic frequencies are almost in the same rate. Fig. 3.16 shows the modified spectrum with EMI reduction. There is no line spectrum and the maximum level of the PWM noise is 210 mV which is about 8% of the normal spectrum and is 22 dB reduction. The spectrum of the conduction noise with EMI reduction is 90 mV which is reduced to 9 % (-21dB). Whole spectrum of the conductive noise with the EMI reduction has the -21dB level of that of the PWM pulse as shown in Fig. 3.15.

The COT pulse modulation is very effective to reduce the EMI noise shown in Fig. 3.16, but it makes the output voltage ripple $\Delta V_o$ increase significantly. The modulated output ripple $\Delta V_{om}$ is 6.0mVpp shown in Fig. 3.17. (The normal ripple $\Delta V_o$ is 1.2mVpp.)

![Figure 3.15 COT control method spectrum without EMI reduction.](image-url)
3.2.3 Improved EMI Noise Reduction with COT Control Method

The COT pulse modulation control method is very effective to reduce the EMI noise shown in Fig. 3.16, but it makes the output voltage ripple $\Delta V_o$ increase very much. We have investigated the improved EMI noise reduction with the COT control method by the phase shift of the comparator output shown in Fig. 3.18. Fig. 3.19 shows the block diagram of the improved EMI noise reduction with the COT converter.
Figure 3.18 Improved EMI noise reduction with the COT control method.

Figure 3.19 Block diagram of improved EMI noise reduction with the COT converter.
Fig. 3.19 shows a block diagram of improved EMI noise reduction with the COT converter. In Fig. 3.13, PWM signal is modulated by tail edge and the output ripple is increased. In Fig. 3.19 we can find that the PWM signal is also modulated by rise edge using phase shift. The output ripple of improved EMI noise reduction with the COT converter shown in Fig. 3.20. The modulated output ripple $\Delta V_{om}$ is 3.3mVpp and smaller than the COT control method with EMI reduction.

![Figure 3.20](image)

Figure 3.20 Output ripple with improved EMI noise reduction with the COT converter.

### 3.2.4 Conventional EMI Noise Reduction with Ripple Injection Method

As we mentioned in Section 2.3.4, the ripple injection method of the hysteretic control converter also has good performance because no need of a hysteresis comparator keeps the high frequency response. In order to generate the large ripple (or the triangular signal) synchronized with the output voltage ripple $\Delta V_o$ or the PWM pulse, the $C_fR_f$ circuit is added across the inductor. This large ripple is injected into the ripple $\Delta V_i$, which is much larger than $\Delta V_o$ and connected to the negative input of the comparator through the coupling capacitor $C_b$. The PWM pulse is easily generated to compare this large signal with the reference voltage $V_r$.

The block diagram of EMI noise reduction with the ripple injection method is shown in Fig. 3.21. The waveform of the COT pulse generator is shown in red border. It consists of a saw-tooth SAW generator, a comparator Comp2 and a COT reference voltage $Vr_{COT}$. The SAW generator includes a switch, a current source $I_{COT}$ and a capacitor $C_{COT}$. The switch is controlled by the positive edge of $V_{comp}$ and resets / starts the SAW signal. The COT pulse is generated by comparing the SAW signal with the COT voltage reference $Vr_{COT}$. Spectrum of the ripple injection method hysteretic
converter is shown in Fig. 3.22. It is about 400mV and very small.

Figure 3.21 EMI noise reduction with the ripple injection method.

Figure 3.22 Spectrum of the ripple injection method hysteretic converter.
3.2.5 EMI Reduction and Output Ripple Improvement with Ripple Injection Method

The ripple injection method is very effective to reduce the EMI noise shown in Fig. 3.22. But it makes the output voltage ripple $\Delta V_{om}$ increase very much shown in Fig. 3.25, which is no good for the voltage regulator. We have investigated the cancellation method to return $\Delta V_o$ level to the normal level. Increase of $\Delta V_o$ is corresponding to the modulation signal $V_m$. The modulated output ripple $\Delta V_{om}$ is 6mVpp, which is about 5 times of the normal ripple (=1.2mVpp). Modification of the COT pulse width $T_{COT}$ changes the duty ratio $D$ of the PWM pulse. In order to cancel the $D$ change, it is effective to modulate the operating period $T_{op}$ reversely against the modulation signal $V_m$.

Fig. 3.23 shows the circuit to cancel the increase of the output ripple, which adds the modulation signal to the ripple generating CR circuit across the inductor $L$. Fig. 3.24 shows the simulation results of the cancellation ripple $V_{oc}$ versus the attenuator gain $A_C$ with the variant modulation signal level $V_m$. This graph shows that the best value is $A_C=0.37$ with each modulation level $V_m$. When $A_C>0.37$, the modulated ripple is over-compensated and its phase is reversed to be shown by the minus voltage.

Fig. 3.25 shows the cancellation ripple $V_{oc}$ compared with the normal ripple $V_o$ and the modulated ripple $V_{om}$. The ratio of the attenuator is $A_C = 0.33$, the cancellation ripple $V_{oc}$ is almost equal to the normal level 1.2 mV. Fig. 3.26 shows the saw-tooth signal which means the operating period, and the inductor current which indicates in proportion to $V_o$. The cancellation ripple $V_{oc}$ is reduced very small but the operating period $T_{op}$ varies according to the modulation signal $V_m$. The spectrum of the EMI noise is almost the same as the one in Fig. 3.22. The optimum attenuator gain of the cancellation signal is $A_C =3.7$ from the simulation result shown in Fig.3.24.
Figure 3.23 Circuit to cancel the output ripple.

Figure 3.24 Cancellation of the output ripple
3.3 EMI Reduction with Soft-Switching Converter

As we mentioned in Section 2.4, soft switching technology can solve the switching loss and switching noise problems in the circuit, and the switching frequency can be greatly increased. In order to reduce the EMI noise, the modulation of the clock pulse is often realized by shaking its phase or frequency. On the other hand, a high-efficiency, low-noise soft-switching converter has also been developed by the Zero Voltage
Switching (ZVS) operation. Although, its EMI noise is relatively small compared to the usual PWM control switching converter, it has to be still suppressed with unnecessary radiation and conduction noises. Therefore, we discuss the EMI noise reduction in the soft-switching converter. The reduction of the EMI noise level is considered by spread spectrum with the phase modulation of the operation signal by not using a fixed clock.

### 3.3.1 Conventional Soft-Switching Converter

Fig. 2.27 shows the circuit of a buck converter with full-wave type voltage-mode resonant converter. The converter consists of power and control stages. The power stage contains a main power switch SW, a free-wheel diode $D_o$, a main inductor $L_o$, an output capacitor $C_o$ and resonant elements which are an inductor $L_r$, a capacitor $C_r$ and a diode $D_r$. The output voltage $V_o$ compared with the reference voltage $V_{ref}$ can generate an error voltage $\Delta V$, which is compared with SAW the PWM pulse is generated. The main switch SW is controlled by this PWM pulse. The SAW generator is triggered by the output of the comparator which detects the resonant voltage $V_r$ and diode voltage $V_d$. When $V_r$ goes across $V_d$, the SAW starts to rise up.

![Figure 3.27 Circuit of the full-wave resonant converter.](image-url)
3.3.2 EMI Reduction with Soft-Switching Converter

Fig. 3.28 shows the EMI reduction circuit of a full-wave resonant converter. In this circuit we shift the start timing of the SAW Generator1 in Fig. 3.27, in order to spread the noise spectrum. We can trigger shifted SAW Generator2 according to the output of Comp2. The SAW generated from Generator2 and the triangular wave signal for phase modulation are compared to trigger the SAW Generator1 for the PWM signal. Thus, the PWM signal is modulated by modulating the off-timing of the SW. Its operation waveform is shown in Fig. 3.29.

![EMI reduction modulation circuit](image)

Figure 3.28 EMI reduction modulation circuit.

![Simulation waveforms](image)

Figure 3.29 Simulation waveforms in EMI reduction modulation circuit.
Table 3.4 Parameter values in simulation.

<table>
<thead>
<tr>
<th>$V_{in}$</th>
<th>$V_o$</th>
<th>$I_o$</th>
</tr>
</thead>
<tbody>
<tr>
<td>10.0V</td>
<td>5.0V</td>
<td>0.25A</td>
</tr>
<tr>
<td>$L_o$</td>
<td>$C_o$</td>
<td>$F_{ck}$</td>
</tr>
<tr>
<td>200μF</td>
<td>470μF</td>
<td>500kHz</td>
</tr>
</tbody>
</table>

We use the simulator SIMetrix-SIMPLIS for circuit simulation with the circuit parameter values in Table 3.4. The spectrum of the standard PWM method buck converter is shown in Fig. 3.4 in Section 3.1.1, while the one of the full-wave type soft-switching converter without EMI reduction is shown in Fig. 3.29 and the one with EMI reduction is shown in Fig. 3.30.

Compared with Fig. 3.4 and Fig. 3.29, although the spectrum of the PWM signal is equivalent in principle, but the basic spectrum is reduced from 3.50V to 2.94V. Next, comparing the EMI reduction effect (Fig. 3.30 and 3.31) in the soft-switching converter. The basic spectrum of the PWM (shown in red) decreases from 2.94V to 1.12V which is 8.4dB reduction. Conduction noise (shown in green) is also reduced from 359mV to 132mV. The operating frequency is changed from 480kHz to 410kHz due to the influence of the frequency modulation.

Figure 3.30 Spectrum of the soft-switching converter output.
3.3.3 Output Ripple Cancelation with EMI Reduction

By phase-modulating the start timing of the SAW in order to spread spectrum to reduce EMI as we mentioned earlier, the duty ratio of the PWM signal is also modulated. Due to this effect, originally the output ripple $\Delta V_o$ in steady-state is about 1.5mV, but in the EMI reduction situation $\Delta V_o$ becomes large as 22mV in synchronization with the modulated triangular signal as shown in Fig. 3.34 (shown in red) and this is a big problem.

Therefore, we discuss how to let the modulated duty ratio keep to original duty ration. The waveforms of output ripple cancelation method are shown in Fig. 3.32. Red line represents the modulated waveforms. In the PWM converter, duty ratio $D$ can be expressed by Eq. 3.7 which is the same as Eq. 2.1. Here $T_s$ is the switching period and $T_{on}$ is the on-period of the switch, while $T_{off}$ is its off-period.

$$\frac{T_{on}}{T_s} = \frac{T_{on}}{T_{on} + T_{off}} \quad (3.7)$$

In the EMI reduction method, the duty ratio is modulated and it leads to $T_{off}$ extended. Since the duty ratio is unbalanced, the ripple cancelation method is to let the operation period $T_{on}$ corrected longer and change to $T'_{on}$, correspondingly the period will change to $T'$, then the modulation is performed to cancel the change of the duty ratio.

The modulation ripple cancellation circuit is shown in Fig. 3.33, where in PWM edge shift modulation part, using triangular compared with SAW (created from original
PWM) can generate a longer PWM period $T'$. Fig. 3.34 shows the simulation results using modulation ripple cancellation circuit. Compared with EMI reduction method (shown in red), using the ripple cancellation method, the output ripple decrease to 3mV (shown in green), which is very small.

![Figure 3.32 Waveforms in the ripple cancellation circuit.](image)

![Figure 3.33 Circuit of the output ripple cancellation method.](image)
For the communication equipment including the radio receiver, it is very important to reduce the radiation noise at the specific frequencies, such as the receiving frequency of the radio receiver by suppressing diffusion of power supply noise. We have proposed the pulse coding technique to create the notch characteristics in the noise spectrum of the switching converter.

In the ripple cancellation circuit, the PWM signal is phase modulated by shifting the optimum stop timing \( V_d = V_r \) of the resonance voltage. As a result, on-timing of the SW for realizing ZVS is delayed, and as shown in Fig. 3.35, the resonant voltage \( V_r \) causes over-resonant even at 120V. This operation is contrary to the basic ZVS operation of the soft-switching converter. Therefore, we consider about a countermeasure that can cancel this over-resonant while keeping EMI reduction and ripple cancellation enabled.

In order to operate ZVS, it is necessary to maintain the resonance voltage \( V_r \) equal to the diode voltage \( V_d \) even during the over-resonant period. At this time, there is a relationship of \( V_r = V_d = V_{in} \). The current of the resonant inductor \( I_{Lr} \) is not allowed to flow to the diode or the load side. As a method of satisfying this condition, it is considered that both ends of the resonant inductor \( I_{Lr} \) can be shorted to maintain the current value of \( I_{Lr} \) and maintain the resonant voltage \( V_r = V_{in} \).

Fig. 3.36 shows a circuit for solving this problem, and Fig. 3.37 shows its operation waveforms. In this circuit, instead of stopping the PWM signal at the original \( V_r = V_d \) timing, short circuit of \( L_r \) with switching to flow the resonant current in the coil itself at resonant stop timing. As a result, the charging current to \( C_r \) is stopped and the resonance voltage is maintained at 0V. The control pulse of SW is canceled (turned off) simultaneously with the on-timing of the PWM signal, and the resonance voltage waveform has no overshoot of the resonance voltage as shown in Fig. 3.37. We can find

Figure 3.34 Output ripple with EMI reduction (red) and ripple cancellation (green).
that the resonant voltage $V_r$ is equal to 15V, and generates the ZVS operation.

Figure 3.35 ZVS operation waveforms at ripple correction.

Figure 3.36 ZVS operation improvement circuit.

Figure 3.37 Waveforms of ZVS operation improvement.
We see in Fig. 3.37 that before SW turn-on, the peak of resonant voltage is still high. The cause of this over-voltage generation is due to the delay time until $L_r$ is shorted after detection of $V_r = V_d$. There are two ways to resolve this problem. We can set $V_d$ to be lower by -5V than $V_r$, or set $V_r$ higher ($V_r' = V_r + 15V$) than $V_d$. The simulation result of the first way is shown in Fig. 3.38. We see that the resonant voltage peak disappears.

![Simulation result of the resonant voltage improvement.](image)

Figure 3.38 Simulation result of the resonant voltage improvement.

Fig. 3.39 shows the spectrum in case that the ZVS improvement method is used. Since we add the ripple correction to the edge modulation and use triangular waveform to shake the PWM signal, the basic spectrum of PWM (shown in red) decreases from 1.12V to 864mV (2.3dB reduction), compared with the EMI reduction method in Fig. 3.31. Also conducted noise (shown in green) is almost the same.

![Spectrum of ZVS improvement circuit.](image)

Figure 3.39 Spectrum of ZVS improvement circuit.

We have proposed the output ripple cancelation method for the EMI reduction full-wave type soft-switching converter, and considered about reducing EMI by modulating the time shift of the resonance end edge. However, the modulation of the resonant operation adversely affects the ZVS operation, and the output ripple also increases; then we add a ripple cancellation circuit. Also the ZVS operation is improved to reduce the EMI spectrum by more than 10dB. Furthermore, the output modulation ripple can be suppressed to 1mV, and EMI and conducted noises also are reduced.
3.4 Summary

This chapter has proposed methods in order to reduce EMI noise for the normal buck converter, hysteretic control converter and soft switching converter.

EMI noise reduction with clock frequency modulation is used by shaking the frequency of the saw-tooth generator. But with this modulation, the output ripple becomes very large, then we created EMI reduction & ripple improvement with saw-tooth correction method to solve this problem.

For the clock-less hysteretic control converter, it is difficult to shake the PWM pulse. We have modified the width of the COT pulse to shake the frequency of the operating pulse to reduce EMI noise, and created the method to cancel the output voltage ripple.

Similarly, soft switching converter is also clock-less converter. EMI reduction with soft switching converter is used by modulating the time shift of the resonance end edge. At this time, modulation of the resonant operation adversely affects the ZVS operation, and the output ripple also increases. Along with this ripple cancellation circuit, the ZVS operation is also improved to reduce the EMI spectrum by more than 10dB. Furthermore, the output modulation ripple can be suppressed.

In the next chapter, we propose an EMI spread spectrum technique with the selectable notch frequencies using the pulse coding methods for DC-DC switching converters.
4. Notch Frequency with Pulse Coding Control

In order to reduce EMI noise, the technique such as a spread spectrum method that randomly modulates the clock signal is being used. This includes using ΣΔ and Δ modulation, instead of conventional pulse width modulation [36]-[37]. However, reduction in peaks comes at the expense of high noise floor due to the quantization noise added by the ΣΔ modulator. This is problematic for many noise-sensitive loads and often mandates using LDOs for post regulation and there is a problem that the diffusion noise is superimposed on an unwanted band (diffusion band shown in Fig. 3.6). Particularly, in the automobile field, the density and complexity of internal electronic circuits are progressing toward electrification and automatic driving. If EMI countermeasures are not taken, noise may be superimposed on the radio band or malfunctions may be induced in other electronic devices.

As we mentioned in Section 1.2.3, we find that the notch characteristics can be applied in DC-DC switching converter to reduce EMI. In this chapter, we propose an EMI spread spectrum technique with the selectable notch frequencies using the pulse coding methods for DC-DC switching converters of communication equipment. The notches in the spectrum of the switching pulses appear at the frequencies obtained from empirically derived equations using the pulse coding method: the PWC (Pulse Width Coding) method, the PCC (Pulse Cycle Coding) method and the PWPC (Pulse Width and Phase Coding) method. We show the relationships between the notch frequencies and the coded pulses in the simulation. We also derived the theoretical formula of the notch characteristic.

4.1 Pulse Width Coding (PWC) Control Switching Converter

As for the pulse coding control method is usually used for the switching converters, it is very important to reduce an Electro Magnetic Interference (EMI) problem, mainly by suppressing the peak level of the fundamental frequency and its harmonic frequencies. Using these methods, the peak levels of the line spectrums are reduced and the energy at the basic frequency and its harmonic frequencies are spread to all frequencies, which would not be desired for the communication equipment such as a radio. Therefore, we researched coding methods that automatically generate notch characteristics in the reception frequency.
4.1.1 PWC Method Switching Converter

In the pulse coding control methods, the main switch is controlled by the pulse coded drive signal PCD which is selected from two coded pulses. Pulse 1 and Pulse 2 are obtained by the pulse coding. These two coded pulses are selected by the select signal SEL supplied from the Flip-Flop as shown in Fig. 4.1. The Flip-Flop and two pulse generators (Pules 1, 2) are triggered by the internal clock. When the SEL signal is High, then the Pulse 1 is selected. When the SEL signal is Low, the Pulse 2 is selected. According to Fig. 4.1, various coding methods can be easily changed only by changing the pulse generation circuit of the coding part.

![Switching converter with pulse coding](image)

**Figure 4.1** Switching converter with pulse coding.

Generally, the control scheme of the switching converter uses a PWM method which linearly modulates the pulse width to feedback. Here, we use the PWC method of discretely modulating the width of the feedback pulse.

Fig. 4.2 shows the control circuit for the PWC method switching converter. The error voltage $\Delta V$ between the output voltage and the reference voltage $V_r$ is amplified and its output logic level is 1-bit high/low signal using a D-type Flip-Flop. This signal is converted to a pulse corresponding to high/low signal by the coding circuit, which is fed-back to the input switch. Fig. 4.3 shows the SEL signal, high voltage $V_H$, low voltage $V_L$ and PWC pulse ($W_H, W_L$). After D-type Flip-Flop, if SEL signal is high, the multiplexer will select $V_H$, comparison with SAW will create $W_H$. If SEL signal is low, the multiplexer will select $V_L$, comparison with SAW will create $W_L$. In order to perform stable control, it is necessary to control the increase and decrease of the output voltage by satisfying the following condition [38]:

$$\text{(Condition)}$$
Here, $D_L = \frac{W_L}{T_{ck}}$ and $D_H = \frac{W_H}{T_{ck}}$ in Fig. 4.1.

In this spread spectrum technology by the PWC method, pulses are generated by digital modulation which converts analog output voltage error to digital signal. By switching these pulses appropriately, the output voltage of switching power supply will be stabilized. As a result, the spectrum of the clock frequency can be spread and the notch can be generated at the arbitrary set frequency.

Parameters are defined to show the empirical formula of the notch frequency of the PWC method. Let $W$ be the width of pulse period, $W_H$ be the longer modulation width and $W_L$ be the shorter one. $N$ represents a positive integer. The notch frequency
\( F_n \) is expressed by the following equation obtained by a numerical experiment [39]-[40]:

\[
F_n = \frac{N}{(W_H - W_L)}
\] (4.2)

It can be seen from Eq. 4.2 that the notch frequency depends only on the difference in the pulse width of the coding signal and does not depend on the clock frequency. By adjusting the pulse width, the notch frequency can be arbitrarily set.

### 4.1.2 Simulation Result with the PWC Control

In this pulse coded control, the output voltage is controlled with only two pulses and there is no need of the saw-tooth signal, but in order to control the output voltage precisely, the frequency of the clock is set to be higher 500 kHz. Other parameters of the switching converter with PWC are shown in Table 4.1.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_i )</td>
<td>12V</td>
</tr>
<tr>
<td>( V_o )</td>
<td>5V</td>
</tr>
<tr>
<td>( I_o )</td>
<td>0.52A</td>
</tr>
<tr>
<td>( L )</td>
<td>200μH</td>
</tr>
<tr>
<td>( C )</td>
<td>470μF</td>
</tr>
<tr>
<td>( T_{ck} )</td>
<td>2.0μs</td>
</tr>
<tr>
<td>( W_H )</td>
<td>1.6μs</td>
</tr>
<tr>
<td>( W_L )</td>
<td>0.3μs</td>
</tr>
</tbody>
</table>

In simulation, we set peak voltage of SAW is 12V. Using voltage-dividing circuit also can manually set \( V_H = 9.6V \), \( V_L = 1.8V \). Correspondingly, using \( V_H \) and \( V_L \) compared with SAW can create \( W_H = 1.6μs \) and \( W_L = 0.3μs \) respectively. Here, the period of the clock signal is given as \( T_{ck} = 2μs \). Fig. 4.4 shows the major signals and Fig. 4.5 shows the spectrum of the coded pulses of the PWC signal. The upward arrows represent clock frequency, twice frequency and three times frequency of the PWC signal spectrum. There appears the notch characteristics frequency \( F_n \) at the frequencies of 770kHz, which are the theoretical frequencies (Eq. 4.2) by calculating from the coded pulses in \( W_H = 1.6μs \), \( W_L = 0.3μs \) situation. The notch frequency also is created at about 1.54MHz which is equal to \( 2F_n \). Since this frequency is partially hidden by high frequency noise of the clock, the notch is not very obvious. As a result, comparing the maximum power of the normal clock in Fig. 3.3 and the proposed circuit in Fig. 4.5, the proposed circuit noise was reduced from 3.5V to 1.1V and a notch is produced. Fig. 4.6 shows the transient response characteristics of PWC method when \( I_o \) change from 0.52mA to 0.72mA. The overshoot was observed.
Figure 4.4 Main signal waveforms of PWC method.

Figure 4.5 Spread spectrum with PWC control.

Figure 4.6 Transient response characteristics of PWC method.
4.2 Pulse Phase Coding (PPC) Control Switching Converter

PPC circuit can be simply realized by a delay circuit and a multiplexer shown in Fig. 4.7. Since the duty ratio of the pulse does not change, it is difficult to satisfy the stability control condition of Eq. 4.1. Therefore, it is inappropriate for the power supply circuit by this system alone, but it can be used for a power supply circuit by using this method with the PWC method combined system.

![Figure 4.7 Buck converter with PPC control.](image)

Parameters are defined to show the empirical formula of the notch frequency of the PPC method shown like Fig. 4.8. Let $\tau$ be the delay of pulse coding, $\tau_H$ be the longer delay and $\tau_L$ be the shorter one. $N$ represents a natural number. This method is classified as one type of pulse period coding (PCC), and the notch characteristics is also expressed by the PCC method Eq. 4.6. Here, consider a pulse train with a clock cycle of $T_o$. Expressing the period $T(k)$ of the $k$-th pulse using the phase by the following Eq. 4.3:

$$T(k) = T + \{\tau(k) - \tau(k-1)\} \quad (4.3)$$

In other words, in the PPC method, the notch characteristics also depend on the previous one pulse. For this reason, the coding cycle $T(k)$ including $2^2$ patterns, and notches are unlikely to occur. To compensate for this, if alternate coding of H/L is performed in phase coding, the following two periodic patterns are available:
\[
T = \begin{cases} 
  T_L = T + \{\tau_H - \tau_L\} \\
  T_S = T + \{\tau_L - \tau_H\}
\end{cases}
\]  \hspace{1cm} (4.4)

Substituting Eq. 4.4 into Eq. 4.6 gives Eq. 4.5 as follows:

\[
F_{np} = \frac{N}{2(\tau_H - \tau_L)}
\]  \hspace{1cm} (4.5)

From this equation, the notch characteristic depends on the twice of difference in pulse phase.

![Waveforms of PPC control](image)

\textbf{Figure 4.8 Waveforms of PPC control.}

\section*{4.3 Pulse Cycle Coding (PCC) Control Switching Converter}

\subsection*{4.3.1 PCC Method Switching Converter}

In the switching converter shown in Fig.4.1, the duties of two coded pulses are different each other in the relationship with Eq. 4.1. In this case, the duty will be changed by changing the pulse period shown in Fig. 4.9.

In Fig. 4.9, there shows the example of two pulses with the PCC method. Here the pulse width \(W_o\) is 0.4\(\mu\)s and the pulse periods are \(T_S=0.5\mu\)s and \(T_L=2.0\mu\)s, then their duties are \(D_H=0.8\) and \(D_L=0.2\). In this case, the equation of the notch frequencies \(F_{nc}\) in the spectrum of the PCD signal is represented below.

\[
F_{nc} = \frac{N}{(T_L - T_S)}
\]  \hspace{1cm} (4.6)
These coded pulses are generated by the circuit which includes the D-Flip Flop (DFF), preset pulse generation counter, differentiator, saw-tooth generator and comparator shown in Fig. 4.10. Pulses with different periods are generated from the next-stage pulse generation counter according to the SEL signal output from the D-FF. Here, $T_L/T_S$ is defined as the pulse period generated corresponding to the high / low of the SEL signal which is the output of DFF. By using a differential circuit, a periodically modulated clock signal can be generated. The generated saw-tooth compared with $V_r$ can create PCC pulse. Figure 4.11 shows the main signal waveforms in the pulse code section of the PCC system. The clock cycle changes according to the SEL signal, and a PCC waveform synchronized with that cycle is output.

![Figure 4.9 Coded pulses with the PCC method.](image)
4.3.2 Simulation Result with the PCC Control

Fig. 4.12 shows the major signals. The pulse lengths of the PCC signal are changed according to the SEL signal. Fig. 4.13 shows the simulation results of the frequency spectrum of the PCC control. In this case, pulse conditions are $T_L=600\text{ns}$ and $T_S=220\text{ns}$,
so the basic notch frequency is calculated as $F_{nc}=2.6\text{MHz}$ from Eq. 4.4. In Fig. 4.13, there appear the notches at around $F_{nc}=2.6\text{MHz}$ but they are not clear. There are many line spectrum because EMI reduction does not use. Appearances of the notch frequencies or the spectrum are easily changed by the conditions of the coded pulse frequencies or the parameters of the switching converter.

Table 4.2 Parameter values of PCC control simulation circuit.

<table>
<thead>
<tr>
<th>$V_i$</th>
<th>$V_o$</th>
<th>$I_o$</th>
<th>$L$</th>
</tr>
</thead>
<tbody>
<tr>
<td>10V</td>
<td>3V</td>
<td>0.5A</td>
<td>100\mu H</td>
</tr>
<tr>
<td>$C$</td>
<td>$W_o$</td>
<td>$T_L$</td>
<td>$T_S$</td>
</tr>
<tr>
<td>470\mu F</td>
<td>170ns</td>
<td>600ns</td>
<td>220ns</td>
</tr>
</tbody>
</table>

Figure 4.12 Simulation waveforms of PCC method.

Figure 4.13 Spectrum of buck converter with PCC control (without EMI reduction).
4.4 Pulse Width and Phase Coding (PWPC) Control Switching Converter

4.4.1 PWPC Method Switching Converter

The configuration of the PWPC method can be easily realized by adding a PPC circuit between the SAW generator of PWC and the clock as shown in Fig. 4.14. In PWPC method, the notch frequency can be realized by Eq. 4.2 and Eq. 4.3, these two equations are made to obtain a large notch. Fig. 4.15 shows the SEL signal and PWPC signal. If select signal is high, $W_H$ will be selected. If select signal is low, shifted $W_L'$ will be selected. Comparing with PWC method, it can be confirmed that the notch characteristics of the PWPC method is deeper.

Figure 4.14 Buck converter with PWPC control.
4.4.2 Simulation Result with the PWPC Control

In the simulation, we set $T_o = 500\, \text{ns}$, $W_H = 320\, \text{ns}$, $W_L = 160\, \text{ns}$, $\tau_H = 80\, \text{ns}$, $\tau_L = 0\, \text{ns}$. Setting to generate large notch at 6.25MHz. Fig. 4.16 shows the simulation spectrum of the PWPC waveform at this time. From Fig. 4.17, the ripple of the output voltage is 20mV (variation: 0.4%) when the current $I_o = 0.5\, \text{A}$. The reason for this ripple we presumed is that a delay component phase was included in the coding signal to control switching. At the same time, no over/under shot was observed for the current change $\Delta I_o = 0.25\, \text{A}$, and the response characteristics are considered to be excellent.
4.5 Derivation of Theoretical Notch Frequency

Until now, the formulas were empirically derived from simulation results. Here, we analyze the various coding methods and derive the theoretical formula for the notch characteristics. In order to get the theoretical formula, we divide the analysis into four steps: 1) Define the waveform of pulse coding method. 2) Fourier transform of defined waveform. 3) Take the absolute value to get the spectral characteristics of the waveform. 4) Get zero point derived from spectral characteristics.

4.5.1 Theoretical Analysis of PWC Method

First, we analyze the PWC method in the single coding method. As shown in Fig. 4.18, we define the PWC signal in one period represent as $T_{ck}$ with two different widths ($W_L$ and $W_H$). The theoretical frequency of the PWC control is derived as Eq. 4.7, performing fast Fourier transforms to the pair of the coding pulses.

$$F(\omega) = \int_{-\infty}^{\infty} f(t)e^{-j\omega t}dt$$

![Figure 4.18 1 period 2 pulse trains of pulse width coding signal.](image)
\[
= \int_{0}^{\frac{W_L}{\omega}} e^{-j\omega t} dt + \int_{\frac{W_L}{\omega}}^{T_c + \frac{W_L}{\omega}} e^{-j\omega t} dt 
\]
\[
= \frac{1}{\omega} \left[ \sin(\omega W_L) - \sin(\omega W_H) + j\cos(\omega W_L) - j\cos(\omega W_H) \right] 
\]
\[
= \frac{1}{\omega} \left[ \sin(\omega W_H) - \sin(\omega W_L) + j\cos(\omega W_H) - j\cos(\omega W_L) \right] 
\]

The left and right sides of the equation are square at the same time:

\[
\omega^2 F^2(\omega) = [\sin(\omega W_L) - \sin(\omega W_H) + j\cos(\omega W_L) - j\cos(\omega W_H)]^2 
\]
\[
\omega^2 |F(\omega)|^2 = 4 \sin^2 \left( \frac{\omega W_H - \omega W_L}{2} \right) 
\]

Take the absolute value of \( |F(\omega)|^2 \) can get the following equation:

\[
|F(\omega)| = \frac{1}{\omega} \left[ \frac{\sin \left( \frac{\omega W_H - \omega W_L}{2} \right)}{2} \right] 
\]
\[
= (W_H - W_L) \frac{\sin \left( \frac{\omega(W_H - W_L)}{2} \right)}{\omega(W_H - W_L)} 
\]
\[
= (W_H - W_L) \sin c \left\{ \frac{\omega}{2} (W_H - W_L) \right\} 
\]

It can be confirmed that the spectrum characteristic of the PWC waveform is a \textit{sinc} function depending on the difference of the pulse widths. In Eq. 4.8, \( \omega = 2\pi f \), and let the frequency at \textit{sinc} function be zero. Then the frequency at zero point is shown as follows [41]-[42]:

\[
F_{\text{notch}} = \frac{N}{W_H - W_L} 
\]

Here, \( N \) is a positive integer. Eq. 4.12 indicates that the notch characteristic is the zero point of the \textit{sinc} function. Notch frequency is decided by the difference of the pulse widths of the coded pulses and does not depend on the clock frequency. By adjusting the pulse width, the notch frequency can be arbitrarily set.

Next, the spectrum characteristics of the eight rows of PWC pulses shown in Fig. 4.19 are calculated using the same calculation method. Assuming that the entire eight trains of pulse have a period \( T_{ck} \), Fourier transform gives Eq. 4.13.
By taking this absolute value, the following Eq. 4.14 is calculated, and by calculating the notch frequency from this equation, the same equation as Eq. 4.12 is obtained.

\[
|F(\omega)| = (W_H - W_L) \sin \left( \frac{\omega}{2} (W_H - W_L) \right) \cdot \sqrt{6 + 4 \cos \left( \frac{\pi}{4} \right) + 4 \cos \left( \frac{\pi}{2} \right) + 4 \cos \left( \frac{3\pi}{4} \right)}
\]

\[
= \sqrt{14} \cdot (W_H - W_L) \sin \left( \frac{\omega}{2} (W_H - W_L) \right)
\]

(4.14)

It indicates that the notch characteristics depend only on the “difference in pulse width” but it is irrespective of the arrangement and number of pulses. Let \( \omega = 2\pi f \), and let the frequency at sinc function be zero. Then the frequency at zero point is shown as follows:

\[
F_{\text{notch}} = \frac{N}{(W_H - W_L)}
\]

(4.15)

It is the same as Eq. 4.12. Fig. 4.20 shows a comparison between the theoretical formula of the sinc function curve and the spectrum of the PWC waveform (pulse width: \( W_H = 3 \mu s, \ W_L = 7 \mu s, \ f_{\text{notch}} = 250 \text{ kHz} \)). From Fig. 4.20, the envelopes of the spectrum are the same as the theoretical formula.
4.5.2 Theoretical Analysis of PPC and PCC Method

Let us analyze the PPC method in the single coding method. As shown in Fig. 4.21, we define the PPC signal in one period represent as $T_{ck}$ with two different phase pulse coding signal ($\tau_H$ and $\tau_L$). The theoretical frequency of the PPC control is derived as Eq. 4.16, performing fast Fourier transforms to the pair of the coding pulses.

$$F_p(\omega) = \int_{-\infty}^{\infty} f(t)e^{-j\omega t} dt$$

$$= \int_{\tau_L}^{\tau_L+W} e^{-j\omega t} dt + \int_{\tau_L+\frac{T_{ck}}{2}}^{\tau_L+\frac{T_{ck}}{2}+\tau_H+W} e^{-j\omega t} dt$$

$$= \frac{1}{\omega}\{ j \cos(\omega(\tau_L - \tau_H)) + \sin(\omega(\tau_L - \tau_H)) - j \cos(\omega(\tau_L - \tau_H - W)) - \sin(\omega(\tau_L - \tau_H - W)) - j \cos(\omega(\tau_H - \tau_L)) - \sin(\omega(\tau_H - \tau_L)) + j \cos(\omega(\tau_H - \tau_L - W)) + \sin(\omega(\tau_H - \tau_L - W)) \}$$

Figure 4.20 Comparison diagram between theoretical formula and spectrum.

Figure 4.21 1 period 2 pulse trains of pulse phase coding signal.
By taking this absolute value, the following Eq. 4.18 is calculated,

\[
|F_p(\omega)| = 2|\tau_H - \tau_L| \sin c \left(2|\tau_H - \tau_L| \frac{\omega}{2}\right) \sin(W \frac{\omega}{2})
\]  
(4.18)

Then the frequency at zero point is shown as follows:

\[
F_{\text{notch1}} = \frac{N}{2|\tau_H - \tau_L|}, \quad F_{\text{notch1}} = \frac{N}{W}
\]  
(4.19)

Here, \(N\) is a positive integer. From Eqs. 4.18 and 4.19, the PPC method depends on two types of \(sinc\) functions and have two types of notch characteristics. This method depends not only on “coding phase” but also on “pulse width”. Here, Eq. 4.18 is the theoretical equation of the PPC method when alternating coding is used.

Next, let us analyze the PCC method in the single coding method. As shown in Fig. 4.22, we define the PCC signal in one period represent as \(T_{ck}\) with two different cycle coding signal (\(T_L\) and \(T_S\)). The theoretical frequency of the PCC control is derived as Eq. 4.20, performing fast Fourier transforms to the pair of the coding pulses.

![Figure 4.22: 1 period 2 pulse trains of pulse cycle coding signal.](image)

\[
F_c(\omega) = \int_{-\infty}^{\infty} f(t)e^{-j\omega t} \, dt
= \int_{0}^{T_{ck}} e^{-j\omega t} \, dt
= \frac{1}{\omega} \left\{ j \cos(\omega T_S) + \sin(\omega T_S) - j \cos(\omega(T_S - W)) \right. \\
- \sin(\omega(T_S - W)) - j \cos(\omega T_L) - \sin(\omega T_L) \\
\left. + j \cos(\omega(T_L - W)) + \sin(\omega(T_L - W)) \right]\} 
\]  
(4.20)

\[
|F_c(\omega)| = 2|T_L - T_S| \sin c \left((T_L - T_S) \frac{\omega}{2}\right) \sin(W \frac{\omega}{2})
\]  
(4.22)
This equation is similar to Eq. 4.18, indicating that the notch characteristic depends on the “coding period” and the “pulse width” as in the PPC method.

### 4.5.3 Theoretical Analysis of PWPC Method

In Section 4.5.2, we found that the frequency characteristics of the PPC and PCC methods were functions that depend on two types of parameters: pulse phase and width. Therefore, the frequency characteristics of the composite coding method, in which two parameters are coded simultaneously, are analyzed mathematically. Next, we analyze pulse width and phase coding (PWPC method), which simultaneously codes pulse width and phase.

![Figure 4.23 1 period pulse trains of pulse width pulse phase coding signal.](image)

As shown in Fig. 4.24, we define the PWPC signal in one period represented as $T_{ck}$ with two types of coding signal. The theoretical frequency of the PWPC control is derived as Eq. 4.23, performing fast Fourier transforms to the pair of the coding pulses.

$$F_{wc}(\omega) = \int_{-\infty}^{\infty} f(t) e^{-j\omega t} dt$$

$$= \int_{\tau_L}^{\tau_L + W_L} e^{-j\omega t} dt + \int_{\frac{T_{ck}}{4}}^{\frac{T_{ck}}{4} + \tau_L} e^{-j\omega t} dt + \int_{\frac{T_{ck}}{2}}^{\frac{T_{ck}}{2} + \tau_L} e^{-j\omega t} dt + \int_{\frac{3T_{ck}}{4}}^{\frac{3T_{ck}}{4} + \tau_L} e^{-j\omega t} dt$$  \hspace{1cm} (4.23)

Eq. 4.24 is the result of taking the absolute value:

$$|F_{wc}(\omega)| = 2|\tau_H - \tau_L| \sin c\left\{2\left|\frac{\tau_H - \tau_L}{2}\right|\right\} \cdot \sin\{W_H - W_L\} \cdot \frac{\omega}{2}$$  \hspace{1cm} (4.24)

In PWPC, it is represented by a sinc function that depends on “pulse width” and “pulse phase”. Since there is a high freedom in setting these parameters, two types of notch characteristics can be generated arbitrarily. Furthermore, if the notch characteristics are set to overlap with $2|\tau_H - \tau_L| = W_H - W_L$, a strong notch characteristic as shown in Eq. 4.25 can be obtained.
\[ |F_{wc}(\omega)| = \frac{\sin^2\left(\frac{\omega}{2}(W_H - W_L)\right)}{\frac{\omega}{2}} \] (4.25)

Fig. 24 shows a comparison of the notch characteristics of Eqs. 4.25 and 4.11. From this figure, it can be confirmed that the vicinity of the zero point (250 kHz) in Eq. 4.25 is wider than in Eq. 11. In other words, the composite coding method has the potential to increase the notch width and improve the depth as well as the single coding method.

Figure 4.24 Comparison of notch characteristics with PWC method and PWPC method.

4.6 Summary

In this chapter we have proposed an EMI spread spectrum technique with the selectable notch frequencies using the pulse coding methods for DC-DC switching converters of communication equipment. The notches in the spectrum of the switching pulses appear at the frequencies obtained from empirically derived equations using many pulse coding method, such as the PWC (Pulse Width Coding) method, the PCC (Pulse Cycle Coding) method and the PWPC (Pulse Width Pulse Phase Coding) method. We show the relationships between the notch frequencies and the coded pulses in the simulation. Also we have derived the theoretical formula of the notch characteristics. In PWC method, the notch frequency depends only on the difference in the pulse width of the coding signal and does not depend on the clock frequency. In PPC method, the notch characteristic depends on the twice of difference in pulse phase. In PCC method, the notch frequency depends only on the difference in the pulse periods. And in PWPC method, the notch frequency depends on “pulse width” and “pulse phase”, and a strong notch characteristic can be obtained.

In this chapter, we manually set \( W_H \) and \( W_L \) to create notch frequency, in the next
chapter, we consider about automatic generation of $W_H$ and $W_L$ to realize an automatic notch frequency generation with PWC control and PWPC control.
5. Full-Automatic Notch Generation of PWC Switching Converter

As we mentioned early, in communication devices such as in-vehicle DC-DC converter, switching frequency and harmonics should not overlap the receiving frequency bands of AM, FM of radio [18]. Let the frequency of the receiving signal from the radio receiver be equal to the notch frequency, and it is possible to greatly reduce influences from other electronic devices. Using the automatic notch frequency generation with the PWC control, the noise near the receiving frequency can be automatically removed. Furthermore, when tuning or switching receiving frequency of communication channels, using the automatic notch frequency generation with PWC control, the notch frequency can be automatically changed. In Chapter 4, we manually set $W_H$ and $W_L$ to create notch frequency; in this chapter, we consider about automatic generation of $W_H$ and $W_L$ to realize automatic notch frequency generation with PWC control and PWPC control.

5.1 Automatic Notch Frequency Generation with PWC Control

5.1.1 Best Relationship Between $F_{ck}$ and $F_n$

Generally speaking, it is the easiest and clearest for the notch frequency $F_n$ to generate at the middle of $F_{ck}$ and $2F_{ck}$ (as shown in Fig. 4.5). When the received signal frequency from a radio receiver is equal to the notch frequency, it is possible to greatly reduce influences on adjacent electronic devices. So we set the notch frequency be equal to the received signal frequency from the radio receiver, that is the input frequency $F_{in}$. The relationship among $F_{in}$, $F_n$ and $F_{ck}$ were shown in Eq. 5.1. Here, $P$ is a positive integer, which determines the notch position, it also guarantees that notch frequency can be generated at input frequency in the high situation. Accordingly, the relationship between the input period $T_{in}$ and the clock period $T_{ck}$ is shown in Eq. 5.2.

$$F_{in} = (P + 0.5) \times F_{ck} \quad (5.1)$$

$$T_{ck} = (P + 0.5) \times T_{in} \quad (5.2)$$
According to Eq. 5.1, in the case $P=1$, the notch frequency $F_n$ can be arbitrarily created between $F_{ck1}$ and $2F_{ck1}$ and equal to $F_{in1}$. In the case $P=2$, the notch frequency $F_n$ can be arbitrarily created between $2F_{ck2}$ and $3F_{ck2}$ and equal to $F_{in2}$ shown in Fig. 5.1.

![Figure 5.1 Best position of $F_n$ occurrence.](image)

On the other hand, the duty ratio $D$ of the PWC signal in the switching converter is usually represented, such as by Eq. 2.6. Moreover, original clock signal shown in Fig. 5.2 means PWC signal with no coded and the pulse width is $T_o$. It also corresponds to Eq. 5.3, here we set $D_o$ to 0.5. We can create pulse-H and pulse-L respectively according to $T_o$ as shown in Fig. 5.2. It also corresponds to Eq. 5.4; here $T_p$ is the pulse difference between $W_H$ and $T_o$ or $T_o$ and $W_L$. The period $T_n$ of the notch frequency was derived from the difference between the pulse widths of $W_H$ and $W_L$ [38]-[39]. In this case, $W_H$, $W_L$ and $T_o$ should have the relation as shown in Eq. 5.5 in order to control the output voltage $V_o$ to be stable. Here $2 \times T_p$ is equal to $T_n$, which means the difference between $W_H$ and $W_L$. 
5.1.2 Automatic Notch Frequency Generate from Clock Pulse

In Eq. 5.2, the period of clock $T_{ck}$ can be generated by measuring the period of the input pulse $T_{in}$. When $P=1$, the notch frequency can be arbitrarily created between $F_{ck}$ and $2F_{ck}$ where we just input $T_{in}$ like Fig. 5.1. In this case, the clock period $T_{ck}$ is shown in Eq. 5.6.

$$T_{ck} = (1 + 0.5) \times T_{in} \Rightarrow T_{ck} = 1.5T_{in} \quad (5.6)$$

And it is easy to realize $T_{ck}$ with a shifter and a digital adder in digital circuit. Fig. 5.3 shows the automatic PWC method pulse coding circuit according to Eqs. 5.3-5.5 in $D_{o} = 0.5$ situation. In this case, $W_{H} = 0.5T_{ck} + 0.5T_{in}$ and $W_{L} = 0.5T_{ck} - 0.5T_{in}$. 

Figure 5.2 Timing chart of relationship between Pulse-H and Pulse-L of PWM signals.

$$T_{o} = D_{o} \times T_{ck} = \frac{V_{o}}{V_{i}} \times T_{ck} = 0.5T_{ck} \quad (5.3)$$

$$W_{H} = T_{o} + T_{p}, \quad W_{L} = T_{o} - T_{p} \quad (5.4)$$

$$T_{n} = W_{H} - W_{L} = 2 \times T_{p} \quad (5.5)$$
Then, let we consider about $P=N$ situation, here $N$ is a positive integer. The notch frequency can be arbitrarily created between $N F_{ck}$ and $(N+1)F_{ck}$. In this case, the clock period $T_{ck}$ is shown in Eq. 5.7.

$$T_{ck} = (N+0.5)T_{in}$$  \hspace{1cm} (5.7)

Fig. 5.4 shows the automatic PWC method in $P=N$ situation. For example when $N=2$, $F_{in}$ is set to 1.25MHz, the clock frequency is automatically calculated as $F_{ck}=500kHz$ and we expect the notch frequency appears at 1.25MHz between the 2\textsuperscript{nd} and the 3\textsuperscript{rd} harmonics of the clock frequency.
5.1.3 Simulation Results with Automatic Notch Frequency Generation

The simulation of automatic notch frequency generation is based on ideal switches. And we use digital circuit to create coding pulse notch generation as shown in Fig. 5.3 when \( P = 1 \) situation. Fig. 5.5 shows the simulation waveforms of pulse-H and pulse-L when we just set \( F_{in} \) equal to 750kHz. The period of the saw-tooth \( T_{ck} \) can be automatically set to 2\( \mu \)s, and comparison between \( V_L \) and \( V_H \) can produce pulse-L and pulse-H automatically. We can find \( W_H = 1.67 \mu s \) and \( W_L = 0.34 \mu s \). According to Eq. 4.2, we expect notch characteristics frequency \( F_n \) at the frequency of 750kHz. The spectrum generated by PWM signal is shown in Fig. 5.6. The notch characteristics can be reflected at 750kHz which is equal to \( F_{in} \). The bottom level of the notch frequency is 1mV. But there is the line spectrum at the frequency of the clock (0.5MHz) which is equal to 900mV and there appear many harmonic spectra. So we consider about using frequency modulation to reduce EMI noise in coding pulse notch generation circuit.
Figure 5.5 Simulation waveforms of Pulse-L and Pulse-H generation in $P = 1$ situation.

Figure 5.6 Simulated spectrum by PWM signal without EMI reduction when $P = 1$ situation.

We use frequency modulation of $F_{ck}$ to reduce EMI like section 3.1.2. The spectrum generated by PWM signal is shown in the Fig. 5.7. The notch characteristics can be clearly reflected at 750kHz which is equal to $F_{in}$. The bottom level of the notch frequency is 1mV and the spectrum of frequency of the clock (0.5MHz) is equal to 20mV which is very small. We found the notch also appeared at $4F_{in}$. In principle,
3MHz frequency is equal to $6F_{ck}$, and also equal to $4F_{in}$, clock signal and input signal overlapped, so notch should not appear at $4F_{in}$. But from simulation, we can find that there was a big notch at $4F_{in}$. The reason why notch appeared at $4F_{in}$ is still unknown, and this will be discussed as future work.

Figure 5.7 Simulated spectrum with EMI reduction in $P = 1$ situation.

Then we consider about $P = 2$ situation. Fig. 5.8 shows the simulation waveforms of pulse-H and pulse-L when we just set $F_{in}$ equal to 1250kHz. We can find $W_H = 1.39\mu s$ and $W_L = 0.6\mu s$. According to Eq. 4.2, we expect notch characteristics frequency $F_n$ at the frequency of 1250kHz. The spectrum generated by PWM signal is shown in Fig. 5.9. The notch characteristics can be reflected at about 1270kHz which is equal to $F_{in}$ and between the 2\textsuperscript{nd} and the 3\textsuperscript{rd} harmonics of the clock frequency.
Figure 5.8 Simulation waveforms of pulse-H and pulse-L generation in $P = 2$ situation.

Figure 5.9 Simulated spectrum with EMI reduction in $P = 2$ situation.

Then we consider about $P = 3$ situation. Fig. 5.10 shows the simulation waveforms of pulse-H and pulse-L when we just set $F_{in}$ equal to 1750kHz. We can find $W_H = 1.29\mu s$ and $W_L = 0.72\mu s$. According to Eq. 4.2, we expect notch characteristic frequency $F_n$ at the frequency of 1750kHz. The spectrum generated by PWM signal is shown in Fig. 5.11. The notch characteristics can be reflected at about 1750kHz which is equal to $F_{in}$ and between the 3rd and the 4th harmonics of the clock frequency.
5.1.4 Automatic Setting Notch Frequency According to Input Frequency

As we mentioned earlier, when tuning or switching communication channels, automatic adjustment to the input frequency change is necessary. If the communication of channel
1 becomes no good, the frequency of channel 2 is switched. In this part, we discuss the automatic adjustment to the input frequency change from channel 1 to channel 2 applied in the radio receiver as shown in Fig. 5.12. Here, we set duty $D = 0.5$, $P = 1$ situation. If we set the input frequency of channel 1 equal to 750kHz, the output of automatic PWC controller can create notch frequency at 750kHz. If $F_{in}$ change to 1250kHz, corresponding $F_{ck}$, $W_H$ and $W_L$ also change. The notch frequency can be created at 1250kHz automatically. The simulated spectrum of the automatic switching for the input frequency $F_{in}$ change from $F_{n1} = 750$kHz to $F_{n2} = 1,250$kHz is shown in Fig. 5.13 and Fig. 5.14. The notch characteristics can be clearly reflected at 750kHz and 1,250kHz respectively which are equal to the input frequency.

Figure 5.12 Block of change channel 1 to channel 2.

Figure 5.13 $F_{in1} = 750$kHz situation.
Response speed and output voltage ripple are also important when tuning or switching communication channels. In the simulation, we alternate the input frequency $F_{in}$ to 750kHz and 1,250kHz at every 250$\mu$s. Correspondingly, the peak voltage and period of saw-tooth SAW are also changed as shown in Fig. 5.15. When $F_{in}$ changes, the transient response of output voltage also changes. The steady output voltage ripple $V_{\text{ripple}}$ is about 1m$V_{pp}$, when $F_{in}$ changes from 750kHz to 1,250kHz, and the overshoot is about 3.8mV. The relationship between $V_{\text{ripple}}$ and $F_{ck}$ in buck converter also can be expressed as Eq. 5.8 [43]. From the equation we can find $F_{ck}$ is inversely proportional to $V_{\text{ripple}}$. According to the simulation results, we can realize automatic switching between two receiving signals with notch characteristics with small output voltage ripple.

$$V_{\text{ripple}} \propto \frac{(1-D)}{8LCF_{ck}^2}$$  \hspace{1cm} (5.14)
Figure 5.15 Automatic switching on transient response and saw-tooth.

According to the simulation results, we can realize automatic switching between two receiving signals with notch characteristics.

5.2 Automatic Notch Frequency Generation with PWPC Control

As we discuss in Section 4.5.3, the coding method combined PWC method and PPC method have the potential to increase the notch width and improve the depth. Now we consider about PWPC method to control switching in order to reduce EMI noise. And also we consider about automatic generation of Pulse-H and Pulse-L and Pulse-LD (Fig. 5.16) to realize automatic PWPC control.

5.2.1 Automatic Method to Generate PWPC Control

In PWPC method, the notch frequency can be realized by Eq. 4.2 and Eq. 4.3, these two equations are made to obtain a large notch. Fig. 5.16 is the configuration of PWPC system. Automatic PWC controller can create $V_H$ and $V_L$, in PWPC method, using $V_H$ compared with saw-tooth can created Pulse-H. Using $V_L$ compared with delayed saw-tooth can created Pulse-LD. Fig. 5.17 shows designed timing in PWPC method, where the phase shift $\tau$ is equal to $0.5T_{in}$ if Eq. 4.2 is equal to Eq. 4.5 in order to create big notch.
Figure 5.16 Pulse coding of PWPC method.

Figure 5.17 Timing chart of buck converter with PWPC control.
The relationship between $F_{ck}$ and $F_n$ are shown in Eq. 5.1. And according to Eq. 5.4, the following equations can be obtained ($P=1$ situation). $P_{LD}$ is timing of rear end of $P_L$.

\begin{align*}
W_H &= T_o + T_p = D \cdot T_{ck} + 0.5T_{in} \\
W_L &= T_o - T_p = D \cdot T_{ck} - 0.5T_{in} \\
P_{LD} &= \tau + T_o - T_p = \tau + D \cdot T_{ck} - 0.5T_{in}
\end{align*}

(5.15)

### 5.2.2 Simulation Results with Automatic Notch Frequency Generation with PWPC Control

Fig. 5.18 shows the waveforms of saw-tooth with period $T_{ck}$ and delay $T_{ck}$. Fig. 5.18 shows the major signal of Fig. 5.16. The coding pulse $P_H$, $P_L$ or $P_{LD}$ are generated by comparing the voltage $V_H$ and $V_L$ with the saw-tooth signal and delayed saw-tooth signal.

In the proposed system, the input/output voltage are $V_{in}=10V$ and $V_o=5V$, so the theoretical duty ratio of the signal is $D=0.5$. When the frequency of the input signal is set at $F_{in}=750kHz$, and in $P=1$ situation, the frequency of the clock is guided at $F_{ck}=500kHz$. In order to set the notch frequency at $F_{in}=750kHz$, the calculated pulse width is $W_H=1.67\mu s$, $W_L=0.33\mu s$, $\tau=0.67\mu s$ according to Eq. 5.15.

![Figure 5.18 Waveforms of saw-tooth with period $T_{ck}$ and delay $T_{ck}$](image)
Seeing the simulation results, the simulated widths of the coded pulses are set to about $W_H=1.67\,\mu s$, $W_L=0.33\,\mu s$, $\tau=0.67\,\mu s$ as shown in Fig. 5.19. In this case, the simulated notch frequency appears at $F_n=750\,kHz$ shown in Fig. 5.20, which is almost equal to the theoretical notch frequency $F_{in}=750\,kHz$. There appears a big notch at $F=3.0\,MHz$, which is the $4^{th}$ harmonic of the fundamental notch frequency $F_n$. We can find double notch creates notch up to high frequencies, and the bottom level of the notch frequency is 1mV.

---

Figure 5.19 Main waveforms of PWPC method.

Figure 5.20 Simulated spectrum with EMI reduction using PWPC method.
5.3 Automatic Design of Duty Ratio $D$ in Full Automatic Notch Frequency Generation

In the previous discussion, we keep setting duty ratio $D$ to 0.5 ($V_i = 10V, V_o = 5V$) in the buck converter. If $D$ is not affected by any factor, $D$ is accurate, the SEL signal (Fig. 4.1) will keep in balance, and the average voltage of the SEL signal $V_{SEL} = \frac{V_{cc}}{2}$.

However, if $D$ shifts, the duty of the SEL signal $D = \frac{V_{SEL}}{V_{cc}}$ will be affected. Then the balance of the inductor current will be shifted and influence the output voltage ripple. Moreover, as the power supply IC, it is necessary to automatically detect or set the condition for $D$ when $V_i$ and $V_o$ change. Therefore, we discuss the method of $D$ setting and automatic detection.

5.3.1 Analysis Relationship Between Conversion Voltage Ration and PWM Duty Ratio

As we mentioned earlier, in the automatic PWC control, just the input frequency $F_{in}$ can create the clock frequency $F_{ck}$ and coding pulses $W_H, W_L$ automatically using the following Eqs. 5.16 and 5.17 according to Eqs. 5.2, 5.4, 5.5 and Fig. 4.2. Here we define that in ideal condition $D_H = D_L = D_P$, $D_P$ is the shift value of $D$, and we set $T_{in} = \frac{2}{3}T_{ck}$ when $P=1$ in Eq. 5.2.

$$W_H = (D + D_H)T_{ck} = DT_{ck} + \frac{T_m}{2} = (D + \frac{1}{3})T_{ck}$$  

$$W_L = (D - D_L)T_{ck} = DT_{ck} - \frac{T_m}{2} = (D - \frac{1}{3})T_{ck}$$  

(5.16)

(5.17)

If $D$ shifts, the duty of the SEL signal $D_s$ will be affected and it will influence the output ripple $\Delta V_o$. When $D$ shifts, the shifted duty ratio $D'$ can be expressed by Eq. 5.18. At the time of IC design, the designer fixed $\frac{V_o}{V_i}$, that is the designer fixed $D$, $D_H$ and $D_L$. Even if IC user changes $F_{in}$, $D_H$ and $D_L$ are still generated automatically by the designer’s circuit. However, when $V_o$ is changed, $D$ will be changed at present and it is different from designed $D$. 

100
For example, in \( T_{in} = 0.67 \mu s, T_{ck} = 1 \mu s \) situation, in our designed circuit, we set \( D = \frac{V_o}{V_i} = \frac{SV}{10V} = 0.5 \). That is, when \( W_H = 0.83 \) and \( W_L = 0.17 \) according to Eqs. 5.16 and 5.17, the duty of SEL signal \( D_s = 0.5 \), the waveform of the select signal select \( W_H \) and \( W_L \) keep in balance. But when \( D \) shifts, \( W_H \) changes to 0.86 and \( W_L \) changes to 0.20; in our designed IC, if the duty of SEL signal \( D_s \) is still 0.5, it will affect the increase of \( W_H \) and decrease of \( W_L \).

In Eq. 5.18, \( \Delta D \) is the shift variation of \( D \). We define the rate of change \( x = \frac{\Delta D}{D} \). At this time, the shifted \( W_H' \) and \( D_H' \), \( W_L' \) and \( D_L' \) can be expressed by the Eqs. 5.19~5.22.

\[
D' = D + \Delta D = D + D \frac{\Delta D}{D} = D(1 + x) \tag{5.18}
\]

\[
W_H' = (D + \Delta D + D_H)T_{ck} \tag{5.19}
\]

\[
D_H' = D_H' - \Delta D \Rightarrow D(1 - x) \tag{5.20}
\]

\[
W_L' = (D + \Delta D - D_L)T_{ck} \tag{5.21}
\]

\[
D_L' = D_L + \Delta D \Rightarrow D(1 + x) \tag{5.22}
\]

Before \( D \) shifts, \( D_s = 0.5 \) and \( D_H : D_L = 1:1 \). That is the select signal select \( W_H \) and \( W_L \) keep in balance. After \( D \) shift, \( D_H' : D_L' \) can be expressed by the Eq. 5.23.

\[
D_H' : D_L' = (1 - x) : (1 + x) \tag{5.23}
\]

The average voltage of the SEL signal \( V_{SEL} \) can be expressed by Eq. 5.24.

\[
V_{SEL} = \frac{V_{cc}}{(1 - x) + (1 + x)} = \frac{V_{cc}(1 - x)}{2} = \frac{V_{cc}(1 - \frac{\Delta D}{D})}{2} \tag{5.24}
\]

According to Eq. 5.24, we can find \( V_{SEL} \) will be influenced by \( \Delta D_o \) and if \( V_{SEL} \) change, the output voltage ripple also increases.

From above discussion we can get that if the duty ratio shifts from \( D \) to \( D' \), \( D_H \) will be changed to \( D_H' \) and \( D_L \) will be changed to \( D_L' \), the select signal select \( W_H \) and \( W_L \) do not keep in balance and it will influence \( V_{SEL} \) from \( \frac{V_{cc}}{2} \) to \( \frac{V_{cc}(1 - \frac{\Delta D}{D})}{2} \), the output voltage also be increased.
5.3.2 Simulation Result with Influence of $D$ Change

According to Section 5.2.1, we can find if the input voltage $V_i$ is changed for the fixed coding pulse $W_H$ and $W_L$, the duty of the SEL signal will change a lot. This change causes a large change in the inductor current $I_L$ and the output voltage ripple $\Delta V_o$. In the simulation, we set $V_{ref} = V_o = 5.0V$, and change the value of the input voltage $V_i$ to 10V and 15V respectively. Correspondingly, $D$ is going to change to 0.5 and 0.33. Fig. 5.21 shows the waveforms of the select signal. We can find that when $D = 0.5$, the waveform of the select signal select $W_H$ and $W_L$ keeps in balance. But in $D = 0.33$ situation, the waveform of the select signal becomes out of balance, and the output of $W_L$ is more than $W_H$. Fig.5.22 shows the simulated voltage ripple $\Delta V_o$ for $D$ changes. We can find that if $D$ changes, the output voltage ripple will be affected.

![Figure 5.21 Waveforms of the SEL signal.](image_url)
5.3.3 Optimal $D$ Setting Method

Let us consider about $D=0.28$ situation. The simulation result is shown in Fig. 5.23. The upper part shows the waveform of the select signal, while the lower part is the output voltage ripple. We can find that $V_o$ increases greatly with one PWM signal on $W_H$ pulse and then gradually decreases with many $W_L$ pulses. The ripple of the output voltage is very large (about 15mV).
The relationship between the input frequency $F_{in}$ and the duty ratio $D$ is shown in Eqs. 5.16 and 5.17. $D$ is limited by $F_{in}$. $D$ need to satisfy Eq. 5.25, or the select signal will be seriously unbalanced and the output voltage ripple will become bigger.

$$D_oT_{ck} + \frac{T_{in}}{2} < T_{ck}$$

$$D_oT_{ck} - \frac{T_{in}}{2} > 0$$

$$0.33 < D_o < 0.67$$  \hspace{1cm} (5.25)

When the value of $D$ is less than 0.33, in control stage, the number of selected signal SEL to choose $W_L$ is increasing. When the value of $D$ is greater than 0.67, the number of selected signal SEL to choose $W_H$ is increasing. As the result, the duty of the select signal will be seriously unbalanced. Therefore, it is very important to keep $D$ between 0.33 and 0.67.

### 5.3.4 Automatic Detection of PWM Duty Method

According to $D$ and Eqs. 5.16 and 5.17, we can create $W_H$ and $W_L$ as shown in Fig. 5.3. At that time, we set $D = 0.5$. After that, if $V_i$ changes, $D$ also changes according to Eq. 2.6. If still the original circuit is used, the number of pulses of $W_H$ and $W_L$ does not change, and it will create error and output ripple. Therefore, using the $D$ automatic detection method to create new $W_H$ and $W_L$ is necessary.

In $D$ automatic detection method, we consider about a method that if the peak voltage of the SAW waveform generated from $T_{ck}$ can be automatically detected and set to the input voltage $V_i$, using this SAW waveform compared with the reference voltage $V_{ref}$. This time, data of sampling is equal to the $D$.

Fig. 5.24 shows $D$ automatic detection circuit, the SAW is generated by a current source, and the frequency of the SAW is $F_{ck}$. A voltage follower can constitute the peak hold circuit, and the peak hold voltage $V_{peak}$ compared with $V_i$ using an error amplifier will create an error voltage. Then using voltage controlled current source lets the error voltage change to the error current to feedback to SAW generation. This time, the peak voltage of SAW is automatically detected and which is equal to $V_i$. At the end, the comparator generates the $D$ detect signal by comparing the SAW and the reference voltage $V_{ref}$ (equal to $V_o$). Fig. 5.25 shows the main signal waveforms of $D$ detection method. In $V_i = 12V$ situation, the peak voltage of SAW will be created at 12V, compared with SAW and $V_{ref}$, and the sampling data is equal to the $D_1$ data. In $V_i = 10V$ situation, the peak voltage of SAW will automatically change to 10V,
compared with SAW and $V_{ref}$, and the sampling data is equal to the $D_2$ data.

**SAW + peak hold part**

**Error amplification**

**Voltage/current conversion**

Figure 5.24 $D$ automatic detection circuit.

![Diagram of $D$ automatic detection circuit](image)

Figure 5.25 Main signal waveforms of $D$ detection method.

![Signal waveforms of $D$ detection method](image)

Using this method, we have realized the full automatic notch frequency generation technology. In this technology, $D$ can be automatically detected when $V_i$ changes. It also can create notch at the input frequency. The simulation result of the full automatic notch frequency generation shown in Fig. 5.26. The simulation parameters have not been changed in Section 5.1.3 except for $V_i$ and do not modulate the clock pulse in order to noise reduction. This time, change $V_i$ to 15V, correspondingly, $D$ can be automatically detected and equal to 0.33. We can find from the simulation results that the notch characteristics can be reflected at 750kHz which is equal to $F_{in}$.  

105
Figure 5.26 Simulated spectrum with full automatic notch frequency generation without EMI reduction.

The waveform of the select signal is shown in Fig. 5.27. Compared with Fig. 5.21 in $D = 0.33$ situation, the waveform of the select signal select $W_H$ and $W_L$ keeps in balance. Output voltage ripple is shown in Fig. 5.28. Compared with Fig. 5.22, the output ripple decreases from 8.5mV to 1.1mV.

Figure 5.27 Select signal waveform with full automatic notch frequency generation.

Figure 5.28 Output voltage ripple with full automatic notch frequency generation.
According to the above discussion, when setting $D$ in automatic notch frequency generation with PWC control, as long as $D$ is satisfied between 0.33 and 0.67 and using $D$ automatic detection method, $D$ can be automatically detected when $V_i$ changes, and it can create notch at the input frequency, while the output ripple also gets smaller.

5.4 Summary

In this chapter, we realized automatic notch frequency generation with PWC control and PWPC control. We proposed a technique to generate the notch characteristics at the desired frequency in the noise spectrum of the switching converter. The clock pulse and the coding pulses are automatically generated and the notch characteristic automatically appears at the input frequency where the notch frequency $F_n$ appears between the clock frequency $F_{ck}$ and its 2nd harmonic or the 2nd and the 3rd harmonics. We have confirmed with simulation that automatic notch generation in noise spectrum of switching converters with the PWC method and PWPC method can be achieved. Also we have implemented a method of automatic switching between two receiving signals, which can realize the automatic adjustment to the input frequency change from channel 1 to channel 2 applied in the radio receiver.

Then we discuss the necessity of duty ratio $D$, and come up with the $D$ automatic detection method to create full automatic notch frequency generation technology. As the result, when setting $D$ in automatic notch frequency generation with PWC control, as long as $D$ between 0.33 and 0.67 is satisfied and the $D$ automatic detection method is used, $D$ can be automatically detected. When $V_i$ changes, it can create notch at the input frequency, and the output ripple also gets smaller.

In the next chapter, we will confirm the notch frequency by the prototype circuit using the pulse width coding method and implementation of the automatic notch frequency generation with the pulse width coding method.
6. Implementation Evaluation on Pulse Coding Controlled Switching Converter with Notch Frequency Generation

In Chapter 4, the notch in the spectrum of the switching pulses was created by the PWC method. In Chapter 5, notch frequency can be automatically set. We have confirmed with the simulation that the proposed technique is effective for noise reduction and notch generation. Also we have implemented a method of automatic switching between two receiving signals, such that if the communication of channel 1 becomes not good, the frequency of channel 2 is switched. In this chapter, we will confirm the notch frequency experimentally with the prototype circuit. We have implemented PWC power supply and confirmed occurrence of notch characteristics by actual measurement. Also we have implemented automatic switching between two different input frequencies.

6.1 Notch Frequency Generation Experimental of the PWC Method Switching Converter

In Chapter 4, we have implemented a method of notch frequency generation using PWC control switching converter in simulation. In this section, we have confirmed the notch frequency by the prototype circuit.

6.1.1 Experimental Method of PWC Control Switching Converter

We have implemented the prototype circuit in converter with PWC control as shown in Fig. 6.1.
We usually use a universal board for implementation experiment. However, using a universal board, wiring is difficult and performance is hard to come out. In recently, PCB board manufacturing is often used, which can reduce the size of circuit board and product costs, improve the quality and reliability of electronic equipment. This time, we created the PWC control DC-DC converter using PCB board with KiCad software.

Fig. 6.2 shows the flowchart for using KiCad software [44]. It can be roughly divided into three parts: Eeschema part, Pcbnew part and Gerbview part. In Eeschema part, we will make the circuit created by simulation and set the footprint for each component. In Pcbnew part, we need create a layout for the board manufacturing company to actually make. When designing DC/DC switching converters, of course their circuit configuration and selection of components are important, but the PCB layout is comparable in importance. Even if the circuit diagram and component values are reasonable, if the PCB layout is not appropriate, not only performance will suffer, but even correct operation may not be possible. Problems originating in the PCB layout include noise in the output (including spikes and oscillation), worsens regulation, and unstable operation. In many cases, these problems can be resolved through appropriate layout, so PCB layout is very important. In Gerbview part, we make the data to actually order from the board company. The PCB board can be obtained by sending these gerb file data to the manufacturer.
Figure 6.2 The flowchart for using Kicad software.
In PWC control DC-DC switching converter, the circuit in Eeschema is shown in Fig. 6.3. Corresponding to Fig. 6.1, circuit is divided into power stage and control stage. The SEL signal, $V_H$, $V_L$, $W_H$, $W_L$ and PWM are shown in Fig. 6.3. Normally, we can generate saw-tooth directly through pulse generator. But attention that saw-tooth can only output up to 200kHz by pulse generator. So we create saw-tooth with period 500kHz like red border in Fig. 6.6 by using saw-tooth generator circuit. Than using generated saw-tooth waveforms compared with $V_H$ and $V_L$ can created $W_H$ and $W_L$ correspondingly. According to SEL signal high and low select $W_H$ and $W_L$, then created PWM signal. Fig. 6.4 shows the completed circuit board. Next, we will test the performance of this circuit board.

Figure 6.3 PWC control buck converter circuit with Kicad.
Figure 6.4 PWC control buck converter PCB board.

### 6.1.2 Experimental Result of the PWC Converter

Table 6.1 shows the parameter values of this switching converter:

<table>
<thead>
<tr>
<th>Parameter values of implementation circuit.</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_i$</td>
</tr>
<tr>
<td>12V</td>
</tr>
<tr>
<td>$L$</td>
</tr>
<tr>
<td>100μH</td>
</tr>
</tbody>
</table>

We have implemented the circuit and measured the waveforms of $W_H$ and $W_L$ as shown in Fig. 6.5 as well as spectrum of the PWC control switching converter as shown in Fig.6.6. The pulse widths were set by ourselves to $W_H = 1.0\mu s$ and $W_L = 0.4\mu s$. Clock frequency appears between the clock and 2$^{nd}$ harmonics of the clock frequency, or between 2$^{nd}$ and 3$^{rd}$ harmonics, 3$^{rd}$ and 4$^{th}$ harmonics of the clock frequency. Substitute the parameter values into Eq. 4.2, 1.66MHz is calculated, which matches the measured result.
Figure 6.5 Waveforms of $W_H$ and $W_L$ in PWC control buck converter.

Figure 6.6 Spectrum of the PWC control switching converter.

6.2 Experimental of Automatic Notch Frequency Generation

In Chapter 5, we have implemented a method of automatic switching between two receiving signals in simulation. In this section, we have confirmed the notch frequency by the prototype circuit.
6.2.1 Experimental Method of Automatic Notch Frequency Generation

In the automatic notch frequency generation method, the circuit of the control stage in using Eeschema is shown in Fig. 6.7. Corresponding to the control stage in Fig. 5.3. We expect just input $F_{in}$, the notch can be automatically create at the position which is equal to $F_{in}$. The relationship between $T_{in}$ and $T_{ck}$ is $T_{ck} = 1.5T_{in}$. In 1.5 times generation circuit (pink border), just input $T_{in}$ can create $T_{ck}$. The waveforms of $T_{in}$, $T_{ck}$, $Q_2$ and $Q_R$ are shown in Fig. 6.8. Then using saw-tooth with period $T_{ck}$ compared with $V_H$ and $V_L$ can created $W_H$ and $W_L$ correspondingly.

![Automatic notch frequency generation circuit with Kicad.](image)

Figure 6.7 Automatic notch frequency generation circuit with Kicad.
Figure 6.8 Main signal waveforms when using $T_{in}$ create $T_{ck}$.

Combined with PWC control buck converter circuit with Kicad shown in Fig. 6.3 and In Fig. 6.7, connect the black point $T_{ck}$, PWM and SEL with each other can create automatic notch frequency circuit.

Fig. 6.9 shows the completed circuit board, where three red wires connect the two boards. Just input $T_{in}$ using pulse generator, we expect to create notch at the same frequency automatically. Next, we will test the performance of this circuit board.
Figure 6.9 Automatic notch frequency generation PCB board circuit.

### 6.2.2 Experimental Result of Automatic Notch Frequency Generation

Table 2 shows the parameter values of this switching converter:

<table>
<thead>
<tr>
<th></th>
<th>$V_i$</th>
<th>$V_o$</th>
<th>$I_o$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>10V</td>
<td>3.5V</td>
<td>0.16A</td>
</tr>
<tr>
<td>$L$</td>
<td>141μH</td>
<td>$C$</td>
<td>570μF</td>
</tr>
</tbody>
</table>

In case 1, we set $P = 1$ in Eq. 5.1, which means that we expect notch to be created between the clock and 2\textsuperscript{nd} harmonics of the clock frequency. We just input $F_{in} = 400kHz$, the clock frequency $F_{ck}$ can be automatically about 267kHz ($T_{ck} = 3.7\mu s$),
and the pulse widths automatically to be $W_H = 3.0\mu s$ and $W_L = 0.7\mu s$ respectively as shown in Fig. 6.10. PWM signal and SEL signal are shown in Fig. 6.11. According to Eq. 4.2, notch can be calculated to 435kHz. From simulation, notch frequency generated at 415kHz shown in Fig. 6.12. From experimental spectrum of automatic notch frequency generation circuit, the appeared notch frequency is about 425kHz, which is fairly equal to the theoretical result in Eq. 4.2, and this notch appears between the clock and 2nd harmonics of the clock frequency.

![Figure 6.10 Experimental waveforms of $W_H$ and $W_L$ ($F_{in} = 400kHz$).](image)

![Figure 6.11 Experimental waveforms of PWM and SEL signals ($F_{in} = 400kHz$).](image)
In case 2, we still set $P = 1$. By just changing input $F_{in} = 600kHz$, the clock frequency $F_{ck}$ can be automatically about 400kHz ($T_{ck} = 2.5\mu s$), and the pulse widths automatically to be $W_H = 2.1\mu s$ and $W_L = 0.6\mu s$ respectively, as shown in Fig. 6.14. PWM signal and SEL signal are shown in Fig. 6.15. According to Eq. 4.2, notch can be calculated to 666kHz. From simulation, notch frequency generated at 610kHz shown in Fig. 6.16. From experimental spectrum of automatic notch frequency generation circuit, the appeared notch frequency is about 666kHz as shown in Fig. 17, which is fairly equal to the theoretical result in Eq. 4.2; this notch appears between the clock and 2$^{nd}$ harmonics of the clock frequency.
Figure 6.14 Experimental waveforms of $W_H$ and $W_L$ ($F_{in} = 600kHz$).

Figure 6.15 Experimental waveforms of PWM and SEL signals ($F_{in} = 600kHz$).

Figure 6.16 Simulation spectrum of PWM signal ($F_{in} = 600kHz$).
Fig. 6.17 Experimental spectrum of PWM signal ($F_{in} = 600\text{kHz}$).

Fig. 6.18 shows the output voltage ripple in case 1; it shows the ripple at 0.16A and the transient response characteristics at 0.41A. The ripple is about $150mV_{pp}$ and 2% of the output voltage and the overshoot is about 60mV.

![Graph showing transient response characteristics](image)

Figure 6.18 Transient response characteristics of the PWC method.

### 6.3 Summary

In this chapter we have confirmed the notch frequency by the prototype circuit using the pulse width coding method, and we have implemented automatic notch frequency
generation with the pulse width coding method. In radio receiver, if the communication of channel 1 becomes not good, the frequency of channel 2 is switched. So we also implemented automatic switching between two different input frequencies.

When designing DC/DC converters, of course the circuit configuration and selection of components are important, but the PCB layout is comparable in importance. Even if the circuit diagram and component values are reasonable, if the PCB layout is not appropriate, not only will performance suffer, but correct operation may not even be possible. Moreover, improper layout will cause problems such as noise and instability. In many cases, these problems can be resolved through appropriate layout. So appropriate layout is very important.
7. Conclusion

7.1 Conclusion

This dissertation describes the results of research on an electromagnetic interference (EMI) reduction in the DC-DC switching converter. Simultaneously, a novel EMI spread spectrum technology is proposed, that does not distribute the switching noise into some specified frequency bands.

In Chapter 1, we introduce the research background of EMI reduction. Based on the background, we describe that the predecessors noticed the notch characteristics appears in the spectrum of the output pulse in the pulse coding system in digital-to-time converter (DTC) circuit. We proposed the objectives of this research are using spread spectrum techniques for EMI reduction with suppressing diffusion of power supply noise and using spread spectrum technique for clock pulse with suppressing diffusion of power supply noise by pulse width coding method.

In Chapter 2, we review the function and operation of basic DC-DC switching converter. Moreover, the principle of the state-space averaging method required to derive the transfer function of the power stage in the buck converter is described. Then, derivation of the transfer function of the power stage in the buck converter using the state-space averaging method. We conclude here that the merit of buck, boost and buck-boost converters are high efficiency, low cost and compact. On one hand, the noise generation is a major disadvantage of the basic DC-DC converter. Also for the hysteretic control, the response is fast, but there are some demerits such as large output voltage ripple and big EMI noise. Soft switching has the great advantage of suppressing switching loss and harmonic noise. On the other hand, since soft switching is realized using the $L$ and $C$ resonance phenomena, increase in conduction loss due to resonance current is an issue.

Chapter 3 found that there are the line spectra at the frequency of clock and many harmonic spectra in the spectrum of the PWM signal in the basic buck converter. So EMI reduction is needed. Then for the basic buck converters, hysteretic control converter and soft switching converter, we proposed new EMI reduction technologies. EMI noise reduction with clock frequency modulation is used by shaking the frequency of the saw-tooth generator. But the output ripple becomes very large with this
modulation. Then we created EMI reduction & ripple improvement with saw-tooth correction method by correcting the duty change of the PWM pulse to solve this problem. For the clock-less hysteretic control converter, it is difficult to shake the PWM pulse. We have modified the width of the COT pulse to shake the frequency of the operating pulse to reduce EMI noise, and created the method by shift the phase of comparator output to cancel the output voltage ripple. Similarly, soft switching converter is also clock-less converter. EMI reduction with soft switching converter is used by modulating the time shift of the resonance end edge. At this time, modulation of the resonant operation adversely affects the ZVS operation, and the output ripple also increases. Along with this ripple cancellation circuit, the ZVS operation is also improved to reduce the EMI spectrum. Furthermore, the output modulation ripple can be suppressed.

In Chapter 4, we propose an EMI spread spectrum technique with the selectable notch frequencies using the pulse coding methods for DC-DC switching converters of communication equipment. We show the relationships between the notch frequencies and the coded pulses in the simulation. Also we derived the theoretical formula of the notch characteristics. In the PWC method, the notch frequency depends only on the difference in the pulse width of the coding signal and does not depend on the clock frequency. In the PPC method, the notch characteristic depends on the twice of difference in pulse phase. In the PCC method, the notch frequency depends only on the difference in the pulse periods. In the PWPC method, the notch frequency depends on “pulse width” and “pulse phase”, and a strong notch characteristic can be obtained. In Chapter 4, we manually set $W_H$ and $W_L$ to create notch frequency.

In Chapter 5, we consider about automatic generation of $W_H$ and $W_L$ to realize automatic notch frequency generation with PWC control and PWPC control. Also we have implemented a method of automatic switching between two receiving signals, which can realize the automatic adjustment to the input frequency change from channel 1 to channel 2 applied in the radio receiver. Then we discuss the necessity of conversion voltage ratio $D$, and come up with the $D$ automatic detection method to create full automatic notch frequency generation technology.

In Chapter 6, we have confirmed the notch frequency by the prototype circuit using the pulse width coding method, and we have implemented automatic notch frequency generation with pulse width coding method. We have also implemented automatic switching between two different input frequencies.
7.2 Items for the Future Study

As we mentioned in Section 5.1.3, using automatic notch frequency generation with PWC control method, the notch characteristics can be clearly reflected at 750kHz which is equal to $F_{in}$. We found that the notch also appeared at $4F_{in}$. The reason why notch appeared at $4F_{in}$ is still unknown, and this will be discussed as future work.

It was understood that the noise component of a specific frequency could be suppressed by using spread spectrum technology. We just consider about letting the frequency of the receiving signal from the AM radio receiver be equal to the notch frequency, and it is possible to greatly reduce influences from other electronic devices. We also need to consider about high frequency notch generation such as FM radio receiver situation (frequency: 76-95MHz). From Eq. 4.2, notch is created at the difference of coding pulse parameter $s$. For example, the broadcast of FM is 90MHz, that is we need create pulse in 10nS. Here, how to create high accuracy pulse is important. Normally, we set $F_{in} < 1.5MHz$, otherwise the accuracy degrades. To generate a notch in the FM radio frequency band, divide the input frequency $F_{FM}$ and then generate a notch with $F_{in} = F_{FM}/64$ as the input frequency; this method can generate a notch with high accuracy up to about 100MHz until now. Higher multiplication notch frequency creation method is under way.
Bibliography


[11] Takayuki DAIMON, Hiroshi SADAMURA, Takayuki SHINDOU, Haruo KOBAYASHI, Masashi KONO, Takao MYONO, Tatsuya SUZUKI, Shuhei KAWAI and Takashi IIJIMA.


[33] 丸山 貴靖, 清水 敏久. 9 kHz~~150 kHz の 周波数帯域に対応した アクティブノイズキャンセラの開発. 修士学位論文, 平成 29 年, 首都大学東京大学.

[34] 富士電機株式会社：「IGBT モジュールの EMC 設計」.


List of Published Papers

Journal Papers


**International Conference Papers**


Technology and Social Science (ICTSS2019), Kiryu, Japan (8-10 May, 2019).


Systems (ISPACS), Xiamen, China (6-9 Nov 2017).


**Domestic Conferences / Seminars**


究者のための異分野学術交流ワークショップ）慶應義塾大学矢上キャンパス（2018年11月3日）。


**Award**
